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International Technology Roadmap for Photovoltaics (ITRPV.net) Results 2010

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1 Executive summary

The International Technology Roadmap for Photovoltaics (ITRPV) organized by the Crystalline Silicon PV Technology and Manufacturing (CTM) Group* aims to inform suppliers and customers about expected technology trends in the field of crystalline silicon (c-Si) photovoltaics and sets a basis to intensify the dialog on required improvements and standards. The present second edition of the ITRPV was jointly prepared by leading European c-Si solar cell manufacturers, module manufacturers, and wafer suppliers. Feedback and input from various institutes, equipment suppliers and providers of production materials was also included. The present publication consequently covers a wider range of the PV value chain compared to the first edition.

Due to the historical learning curve as well as industry growth, the specific costs per Watt peak (Wp) of PV modules are expected to decrease by 8%-12% per year. This corresponds to a significant cost reduction per module. To reach this purpose, current technology will be optimized, but new technologies also need to be implemented in production between 2013 and 2015.

Detailed requirements for c-Si solar cell manufacturing such as more effective use of material, more productive manufacturing equipment and more advanced processes are given in key parameters. This not only affects the cell production but also the complete value chain. One example is the wafer dimension: to be able to handle thinner and larger wafers, not only the method of making the wafer needs to be modified, but also the cell process and the technology to build the module - rear contact cells will probably be used. In case of cell size the inverter also needs to be adapted to a new current/voltage range.

The roadmap activity is carried out in cooperation with SEMI PV Group and updated information will be published each year in Spring to ensure good communication between manufacturers and suppliers throughout the value chain. More information is available on www.itrpv.net.

CTM Group

The Crystalline Silicon PV Technology and Manufacturing (CTM) Group is a special interest group of Bluechip Energy, Bosch Solar, Q-Cells, SCHOTT Solar, Solarworld, Solland, Sovello, Sunways, Systaic Cells represented by SEMI / PV Group.

2 Approach

It has been essential to gather data for the roadmap. The participating companies active along the value chain from crystallization to the building of modules jointly agree on the parameters to be reported in the roadmap publication. Data preparation is done by anonymously summarizing the input of each company. The expected trends up to the year 2020 are shown in graphs and for some parameters color marking is used to indicate the maturity of the technology today (see Table 1). All parameters are median values and answers are given based on data from the latest generation production line.

The topics are split into three areas: materials, processes and products. Within these groups we will discuss details for wafer, cell and module respectively.

Table 1: Color marking

Green	Industrial solution exists and is being optimized in production.
Yellow	Industrial solution is known but not yet in production.
Orange	Interim solution is known, too expensive or not suitable for production.
Red	Industrial solution is not known.

2.1 Materials

Requirements and trends concerning raw materials and consumables used within the value chain are described in this section. A replacement of some materials will be necessary to secure availability, avoid environmental risks, reduce costs and increase efficiency. Price development plays a major role in reaching the goal of grid parity and is discussed for selected topics.

2.2 Processes

To reduce production costs, new technologies, materials and highly productive equipment including Statistical Process Control (SPC) are needed. By giving information on important key figure of production, as well as details of the process to increase the cell efficiency and finally the power output of the modules, the roadmap will be the guideline to support these developments. In the process chapter we identify manufacturing and technology topics for each section of the value chain. Manufacturing focuses on increased productivity while technology developments have to ensure higher cell and module efficiencies.

Experience from the past and also from other industries shows that it takes about 3 years to implement a new process and new tools in production. The latest example of this in the PV industry is the implementation of chemical rear side etching as a method to isolate the front and rear side. There are two significant hurdles to reach a stable high volume production: first reaching a stable process for some hundred cells in an alpha phase and secondly, for some hundred thousand cells in a beta phase. Only if this has been shown, a process should be implemented in a high volume production, which means that tool manufacturers need to develop alpha and beta tools and qualify the process on these tools before introducing first production tools into the market.

This is directly comparable to the semiconductor industry / ITRS roadmap as shown in Fig. 1 [1].

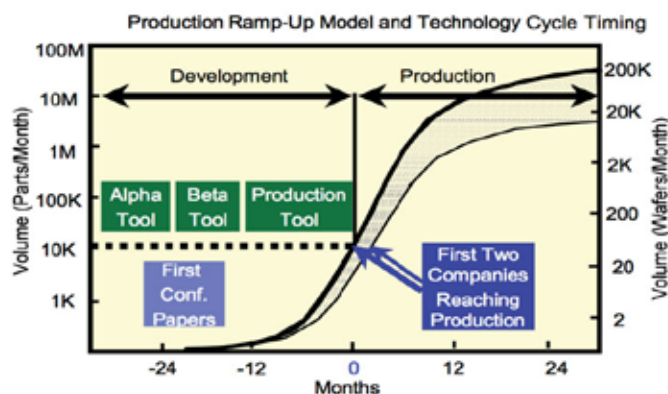


Fig. 1: Typical ramp up model from semiconductor industry / ITRS, an alpha and beta tool is tested before the first two companies reach high volume production with process and production tool (ITRS).

2.3 Products

Each part of the value chain has its respective final product. The chapter “Products” discusses the development of the key features for wafers, c-Si solar cells, and modules over the next decade.

3 Cost reduction

The overall aim of the industry is to reduce the cost of solar generated electricity. The historical learning curve shows that cost of solar modules were reduced by about 17%-26% (learning rate) while the cumulated produced volume was doubled [2-4]. We calculated a scenario for the time period 2010-2020. In this scenario an average yearly industry growth rate of 35% and a learning rate of 20% are assumed. As shown in Fig. 2 this leads to yearly cost reductions of 8%-9% per year for module manufacturing costs on a per piece basis (red line) and of 9%-10% on a per Wp basis (blue line).

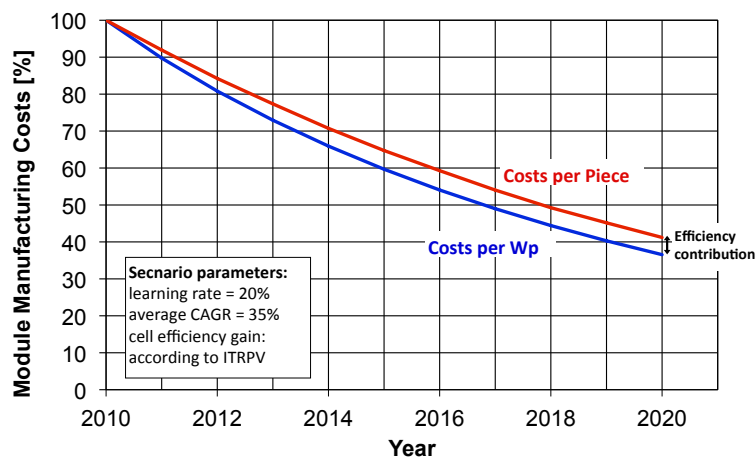


Fig. 2: Modeled module manufacturing costs based on an empirical learning curve with a learning rate of 20%. The cell efficiency gain is assumed to correspond to the values shown in Fig. 28 of this document. It can be seen that costs need to be reduced per piece and not only per WP.

The efficiency data used in Fig. 2 are for 156x156 mm² multicrystalline cells and are taken from Fig. 28 of this document. Fig. 2 demonstrates clearly that the reduction of manufacturing costs per Wp are dominated by the reduction of the manufacturing costs per piece of wafer, cell, and module (assuming a constant cell area) while the contribution of increased cell efficiency is less pronounced. Only a combination of increased module conversion efficiency and significantly reduced manufacturing costs will enable the PV industry to reach the overall cost targets.

4 Results 2010

4.1 Materials

4.1.1 Materials Crystallization and Wafering

The costs for the material have a significant influence on the total costs. To be able to reach the overall goal of cost reduction the price of silicon needs to be reduced by 50% until the year 2020 as shown in Fig. 3.

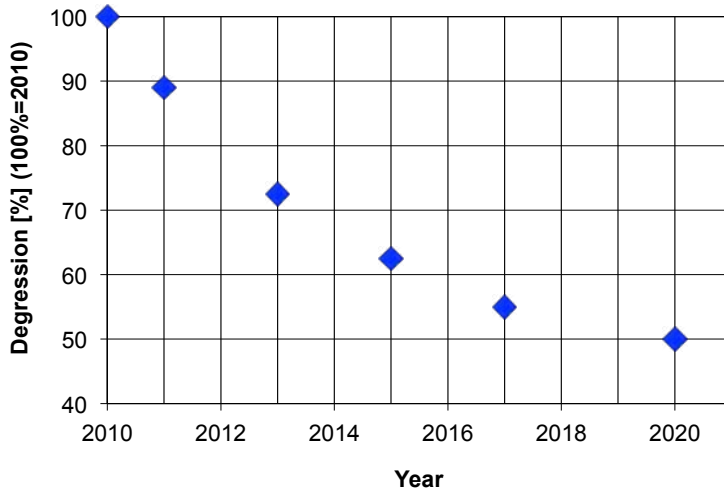


Fig. 3: Required price degression of pure poly-silicon. The chart does not include availability-related fluctuations.

Further setscrews for cost reduction in crystallization and wafering are in the field of consumables such as crucibles, graphite parts, slurry and sawing wires. Fig. 4 shows the required trend of the pricing to reach the cost targets of 50% in 2020. The curve implies a price reduction for these goods of about 7% per year.

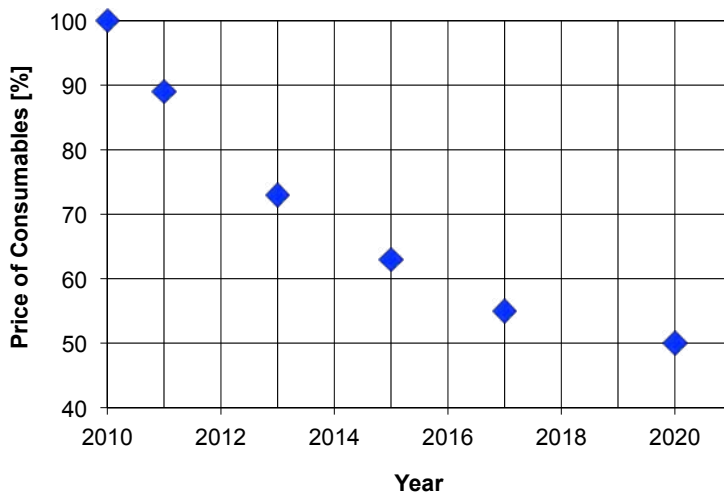


Fig. 4: Required price degression of consumables for crystallization and wafering.

4.1.2 Materials Cell processing

The most expensive material in cell processing is the silicon wafer. Thus reducing the wafer thickness reduces the material cost. Wafers will become thinner, though not as fast as predicted in the first roadmap edition. Fig. 5 shows the expected trend of thinnest wafers processed in mass production. Thickness reduction is postponed by 2 years compared to the first edition, mainly because the higher availability of silicon feedstock led to a significant reduction of wafer prices and reduced the pressure to minimize silicon consumption. Wafers with the current standard format (156x156 mm²) remained the norm until 2020; larger wafers (210x210 mm²) are expected to appear in production earliest 2017.

Slicing of 100 µm wafers is possible from the point of wafer slicing technology but with an unacceptable yield loss so far. The red color-coding in Fig. 5 addresses this issue.

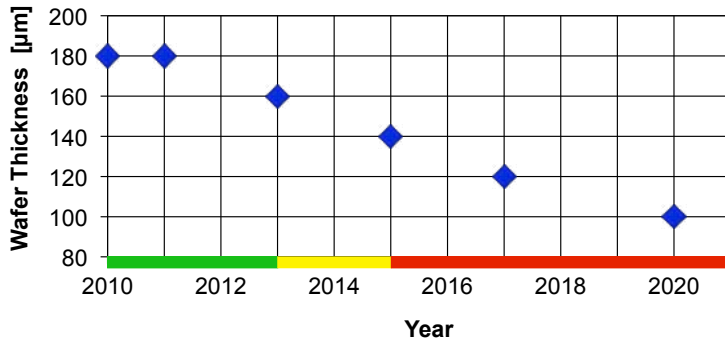


Fig. 5: Trend of minimum wafer thickness processed in mass production of solar cells.

Wafer thickness reduction has the following implications:

1. Cost reduction through reduced wafer pricing by reduction of poly-silicon use.
2. Need for innovative handling concepts for thinner wafers to reduce wafer breakage.
3. Need for new cell concepts suitable for achieving high efficiencies on thin wafers.
4. Need for new interconnection and encapsulation concepts suitable for thin wafers.

Metallization pastes/inks are the most process critical and expensive materials in cell production besides the wafer itself. In industry average, best results are obtained with pastes/inks containing lead. Substituting these pastes/inks by lead-free products is highly requested by the cell manufacturers but will only happen if it can be done without performance loss. The paste suppliers are strongly encouraged to develop lead-free pastes with the same or even better efficiency. The first high-efficiency, lead-free pastes need to be available starting mid 2012 in order for lead-free cells and modules to be commercially available in 2013.

Silver and aluminum are identified as a major cost driver in the metallization process. Therefore paste consumption needs to be reduced in a first step. Fig. 6 shows our estimations for the reduction of silver for 156x156 mm² cells. In a second step silver shall be replaced on a large-scale basis starting in 2015. Cu is intended to be the substitute.

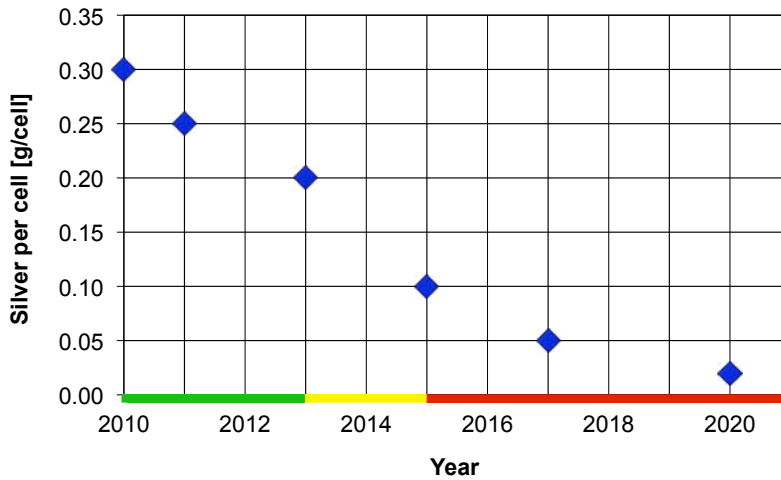


Fig. 6: Remaining portion of silver per cell. A technological development in 2015 is expected to replace silver with Cu.

4.1.3 Materials Module

Looking at the module cost structure there are also materials that need to be improved in performance and reduced in price. The reflectivity at the front side of the glass-air interface will be reduced from typically 4% to 2% by introducing anti-reflection glass from 2013 onwards into the mainstream as shown in Fig. 7. The absorbance in glass and encapsulant need to be reduced to minimize the cell-to-module power loss. This is particularly necessary for blue light due to the improved spectral response of solar cells in that region of the spectrum (see also section 4.2.2).

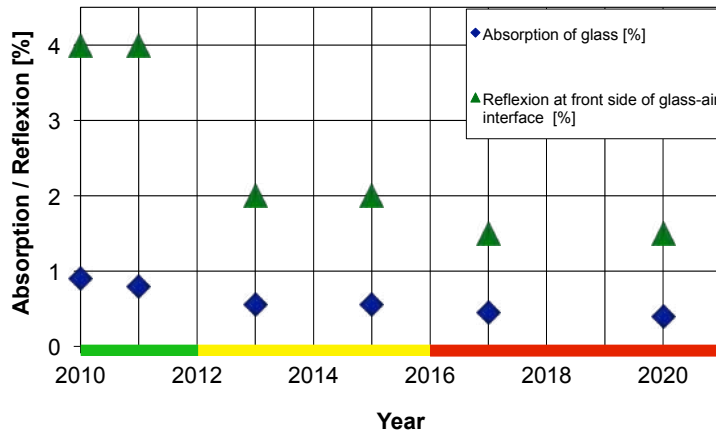


Fig. 7: Requirements for the absorption of glass, as well as reflection at the front side of the glass-air interface.

The consumables frame, glass, encapsulant, back sheet foil and junction box have about equal cost contributions in the distribution of costs. All materials should therefore contribute equally to the ongoing reduction in module manufacturing costs.

4.2 Processes

4.2.1 Processes Manufacturing

Increasing the throughput of the crystallization process is possible by changing common formats of the ingots. The roadmap predicts an increase in ingot mass for monocrystalline silicon (mono-Si) and for multicrystalline silicon (mc-Si) (see Fig. 8). In addition, the ingot height as well as the ingot footprint for mc-Si will rise respectively as shown in Fig. 9 and Fig. 11

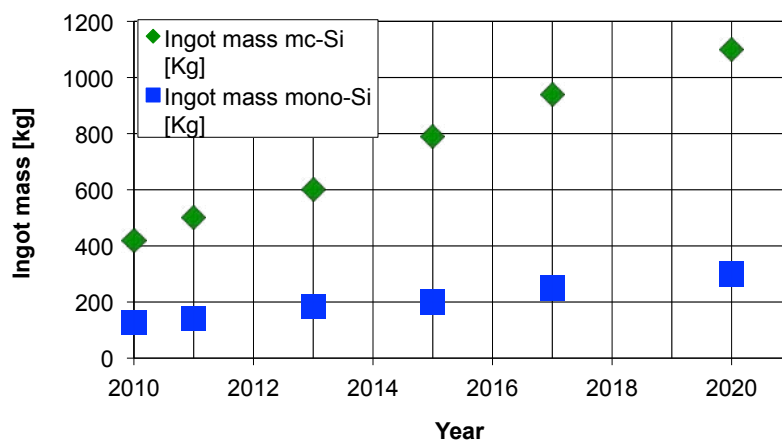


Fig. 8: Trend for ingot mass for mc-Si and mono-Si material.

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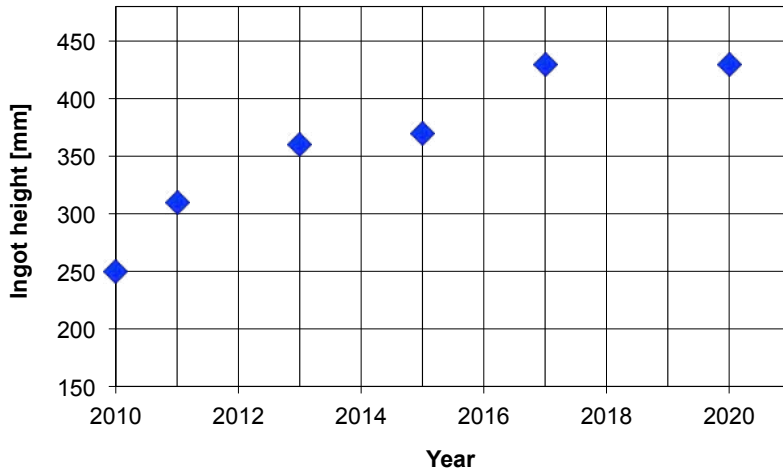


Fig. 9: Trend of ingot height for mc-Si material.

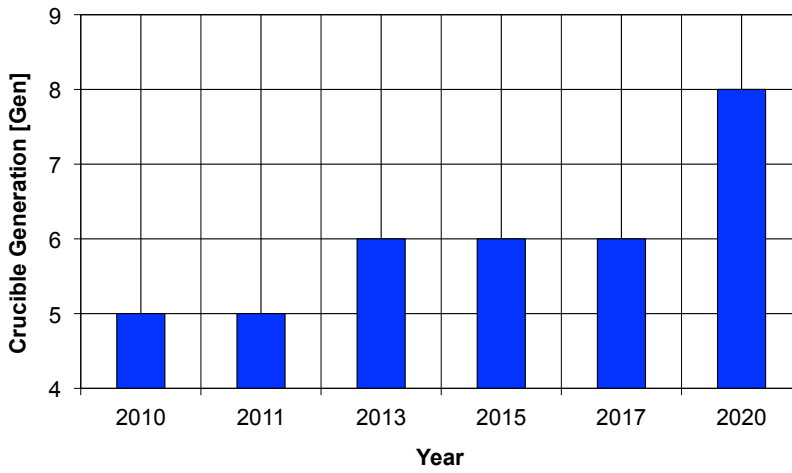


Fig. 10: Trend of mc-Si ingot footprint showing the type of crucible generation used in the newest production lines (mc-Si only).

According to the economy of scale the productivity of tools needs to improve by increasing yield and throughput of a production line resulting in the reduction of labor cost and tool cost per product. This trend is visible when looking at the manufacturing process of ingot growth, wafer sawing, and wafer cleaning. In the areas of sawing and cleaning a 50% increase in throughput is expected as shown in Fig. 12 and Fig. 13 respectively.

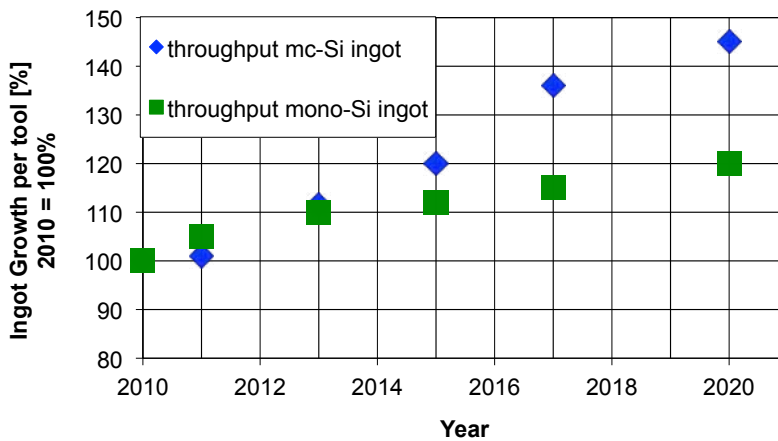


Fig. 11: Throughput per tool for ingot growth.

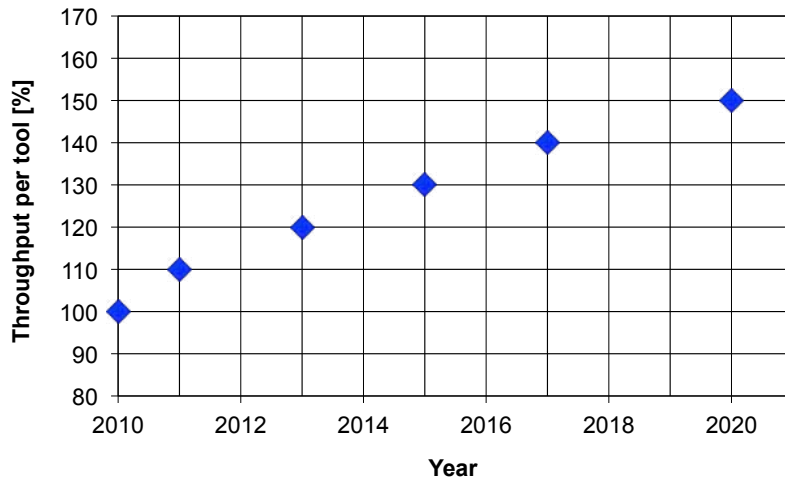


Fig. 12: Throughput per tool for wafer sawing and wafer cleaning processes.

Fig. 13 shows that by 2020, mechanical yield loss in the cell production is expected to decrease to below 1%. Note that, at the same time, this includes introduction of thinner wafers.

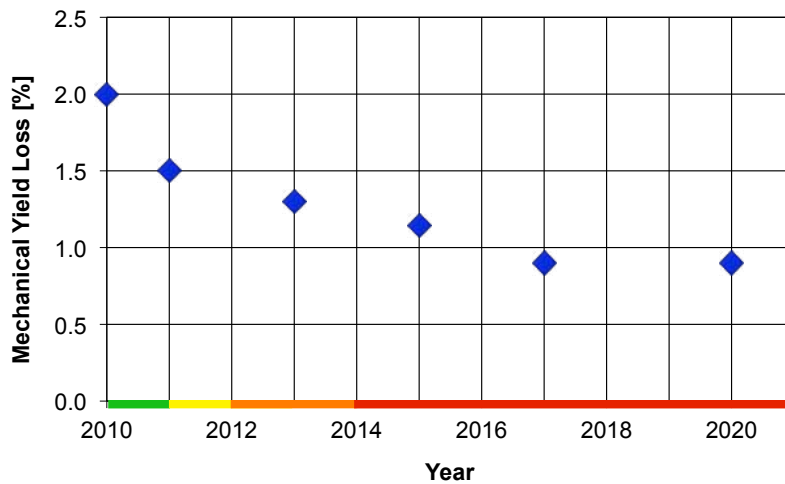


Fig. 13: Mechanical yield loss during cell processing needs to be reduced significantly over the next years.

The tool uptime based on the SEMI Standard E10 is another important factor for optimizing the production lines. To enable uptimes of above 96% as shown in Fig. 14, there is a particular need for improvements in the process groups metallization and classification. Those values have to be seen as minimum requirements – even tools with higher uptime values are preferred.

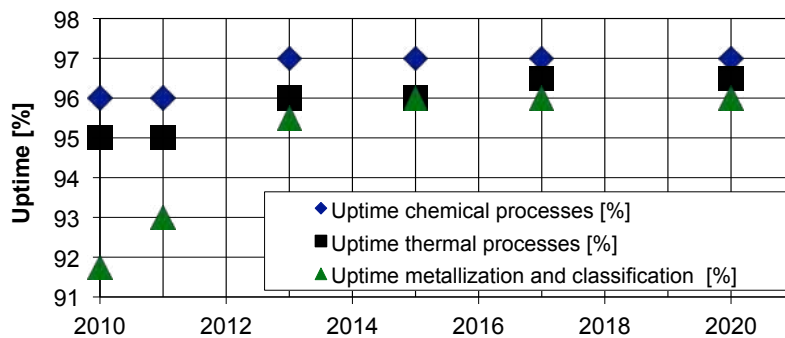


Fig. 14: Tool uptime needs to be improved. There is a high potential for improvements in the metallization and classification process group.

A suitable way to reduce the tool cost per cell is to increase the throughput of the systems. To match throughput in a cell production line the front end (chemical and thermal processes) and back end (metallization and classification) should have equal capacity.

In table 2 we show the expected throughput values with synchronized front-end and back-end processes. A conversion in 2015 to advanced metallization technologies should close the current gap.

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Table 2: Expected throughput of production tools. Front- and back-end tool throughput are expected to match at 1:1 in 2020. All numbers are to be seen as minimum requirements for a high-end production environment.

Year	Front end [wafer/h] (chemical + thermal)	Single line back end [wafer/h] (metallization + classification)
2011-2012	3600	3000
2013	5000	3600
2015	6400	5400
2020	7200	7200

As tool uptime and throughput in cell production are increased, the relative number of operators in relation to the line output will be reduced. We expect a reduction of about 40% as shown in Fig. 15.

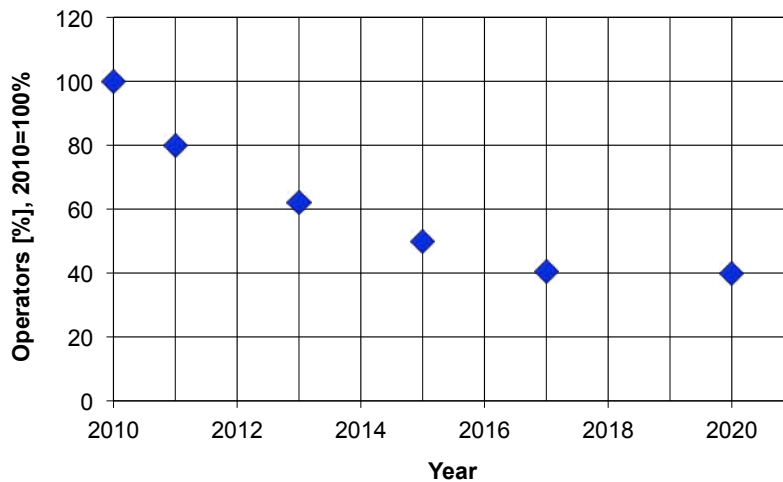


Fig. 15: The relative number of operators needed in a state of the art cell production line can be reduced as tool uptime and throughput increases.

Fig. 16 shows the expected reduction of invest for new cell fabs per MWp as result of the improvements in manufacturing technologies and equipment. This data is based on the input from the participating cell manufacturing companies.

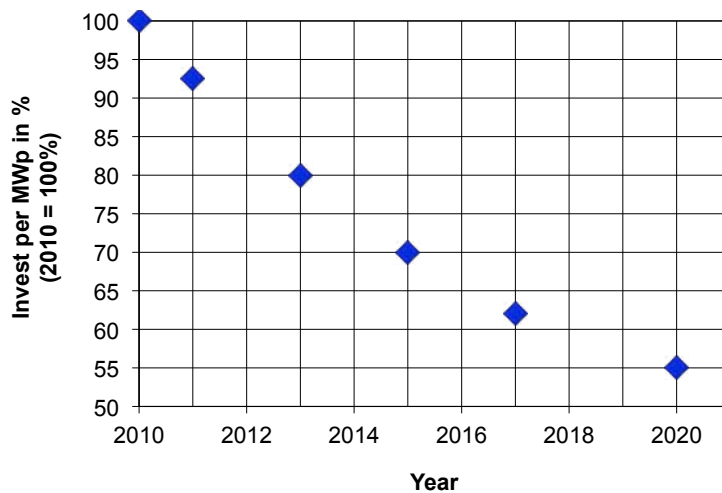


Fig. 16: Chart showing the relative invest per MWp for a c-Si cell production line.

The basis of this estimation is current cell concepts with a comparable or only slightly increased number of process steps. The trend supports the cost reduction requirements discussed in chapter 3 (see Fig. 2) and fits to the assumptions discussed by equipment manufacturers [5] predicting cost savings of about 20% between 2010 and 2013 for new facilities.

Similar trends are predicted in module manufacturing. The expected yield trend in module manufacturing (ratio of good cells in good modules out to good cells in), is shown in Fig. 17. It implies continuous improvements, despite ongoing wafer thickness reductions. In order to process <150 μm thick cells with >99.3% yield from 2015 onwards, a dramatically improved interconnection technology is needed as well as stress-relieving supporting structures.

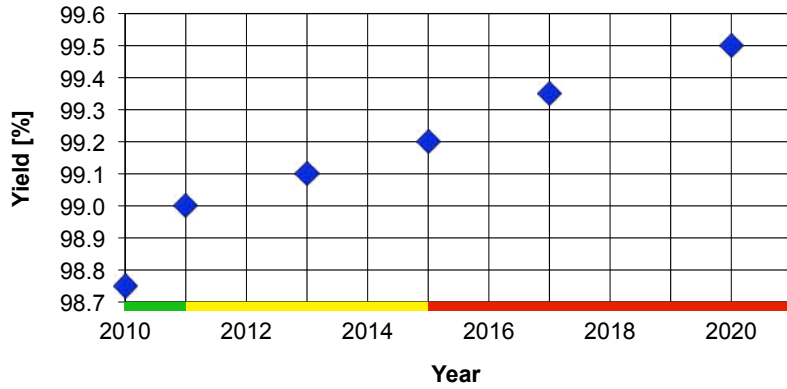


Fig. 17: Expected yield trend in module manufacturing (ratio of good cells in good modules out to good cells in).

To achieve the required cost reductions, module-manufacturing equipment should occupy less floor space (see Fig. 18) and have a higher throughput. A higher throughput can be achieved by a combination of continuous improvement and new developments, particularly for the interconnection and encapsulation processes. For the latter process new encapsulant materials with shorter processing times are desired. For the interconnection process a significant improvement is expected after 2015 when a new interconnection technology and back-contacted cell concepts will be introduced (see Fig. 19).

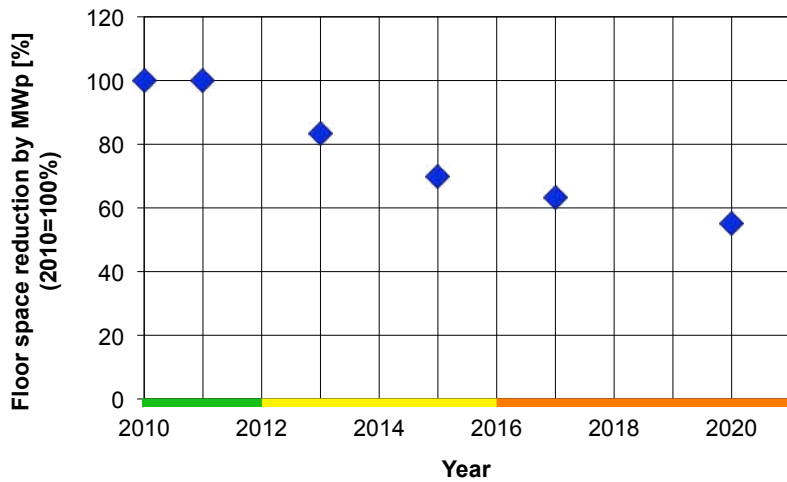


Fig. 18: Expected floor space reduction per MWp output in module manufacturing equipment

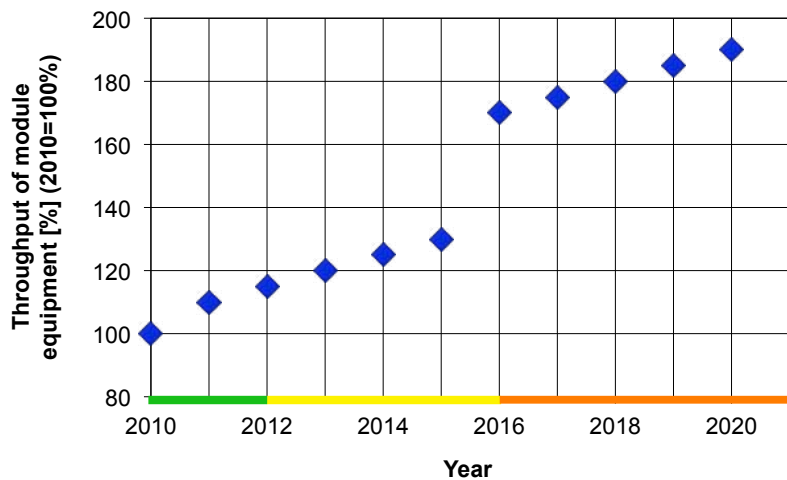


Fig. 19: Expected improvement in throughput of module manufacturing equipment.

4.2.2 Process Technology

Besides production parameters the efficiency is also expected to improve. In the following we indicate necessary process parameters that are mandatory to achieve this improvement.

One essential requirement for thinner solar cells (Fig. 20), reflecting the needs from cell production point of view is the reduction of Total Thickness Variation (TTV).

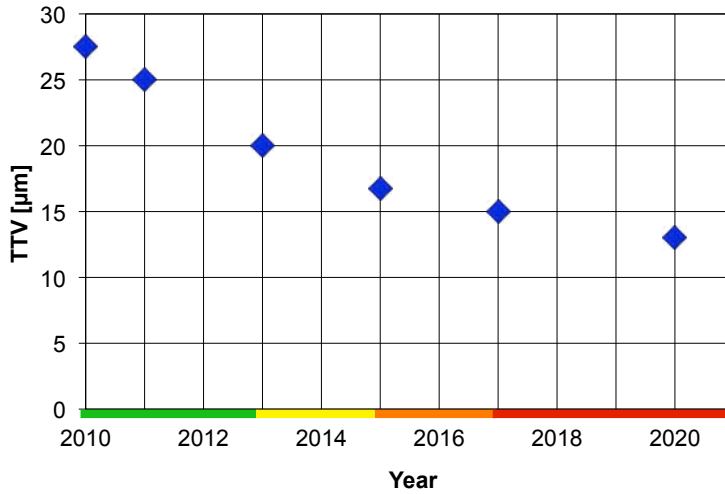


Fig. 20: Expected trend of TTV.

Another challenging parameter as shown in Fig. 21 is the kerf loss. Following the wafer thickness reduction the kerf loss must also be decreased accordingly to achieve a significant reduction in silicon consumption.

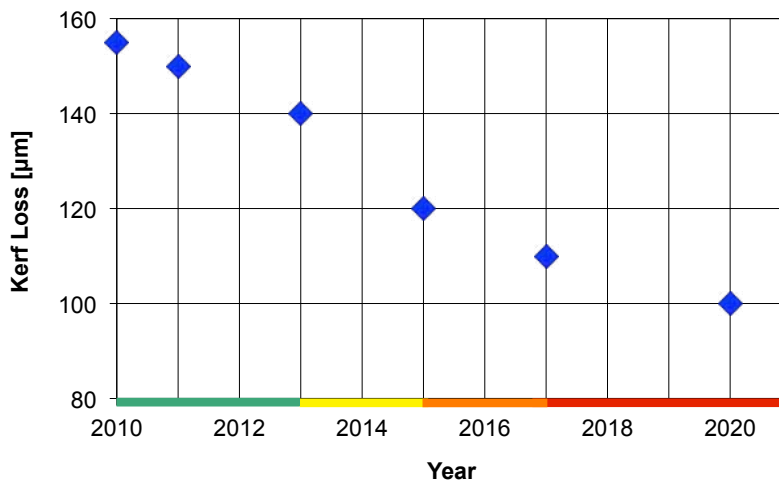


Fig. 21: Kerf loss reduction trend expected by the roadmap.

Solar cell recombination losses in at front and rear side of the crystalline Si bulk material, must be reduced. A reasonable way to describe the recombination losses are the recombination currents $J_0\text{bulk}$, $J_0\text{front}$, $J_0\text{rear}$ that describe the recombination losses in the volume, at the cell front side, and at the cell rear side respectively. Fig.22 shows that all recombination currents need to be reduced.

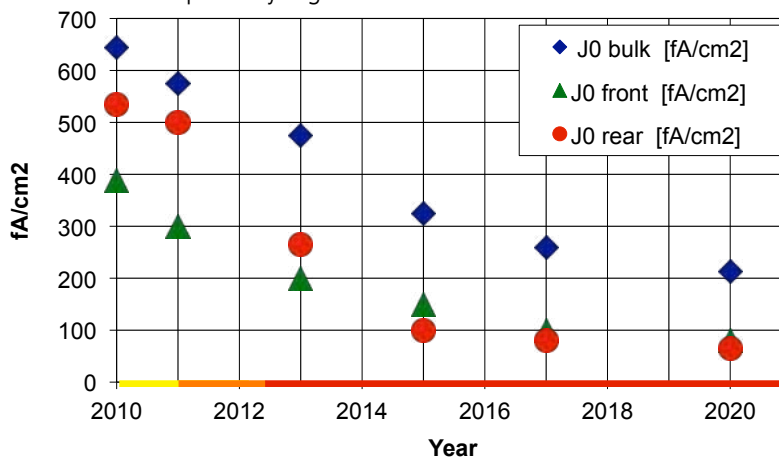


Fig. 22: Trend of recombination currents $J_0\text{bulk}$, $J_0\text{front}$, $J_0\text{rear}$.

The recombination current can be measured as described in literature [6] or extracted from the IV curve, if other J_0 components are known. By 2012 new processes with lower Cost of Ownership (CoO) and better passivation properties, compared to current technologies, will be needed. Values below 200 fA/cm^2 cannot be reached with an Al Back Surface Field (BSF). In addition rear side reflection also needs to improve.

Another parameter influencing recombination losses at the front surface is the emitter sheet resistance. The expected values for n-type emitters are shown in Fig. 23. In case of a selective emitter the sheet resistance shall refer to the lower doped region whereas $J_{0\text{front}}$ includes all relevant front side parameters (emitter, surface, contacts).

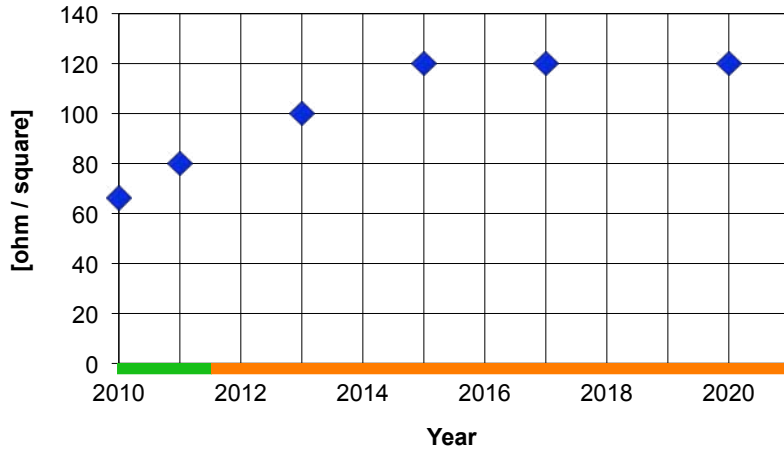


Fig. 23: Emitter sheet resistance will increase.

Front metallization is a key process in the production of c-Si solar cells. A reduction of the finger width is needed, without significantly higher finger resistance. Furthermore the contact to a shallow emitter must to be reliably established. One possibility is the use of a selective emitter structure, but this needs to be done without increasing processing costs. Fig. 24 shows that the reduction of finger width to $80 \mu\text{m}$ seems feasible with current technology. From 2013 on, new and economically feasible solutions are required.

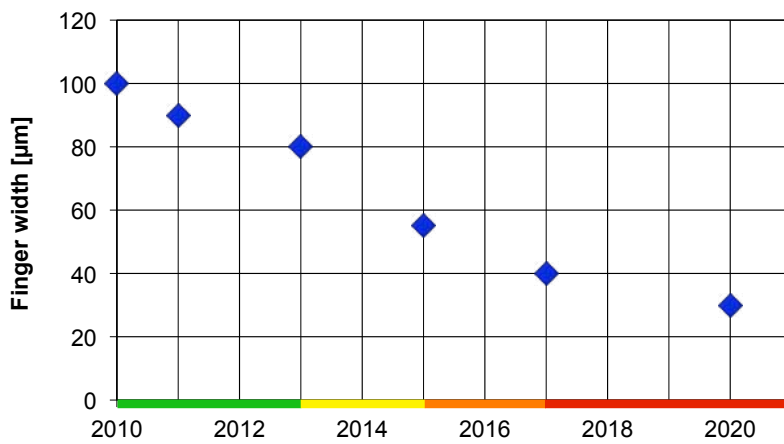


Fig. 24: Finger width needs to be reduced without a significant reduction in conductivity.

A technology change in the metallization process that enables higher throughput and finer line printing and line width is estimated to be introduced in production in 2015. At the same time, the replacement of silver printing (bridge technology) by copper plating (main reason is costs) is expected to take place in order to reduce process costs.

It is important, especially for the front contact, that the alignment precision will improve. With current screen printing technology approximately $30 \mu\text{m} - 50 \mu\text{m}$ can be achieved. As shown in Fig. 25, for more complex cell structures, by 2015 the total accuracy needs to be better than $10 \mu\text{m}$.

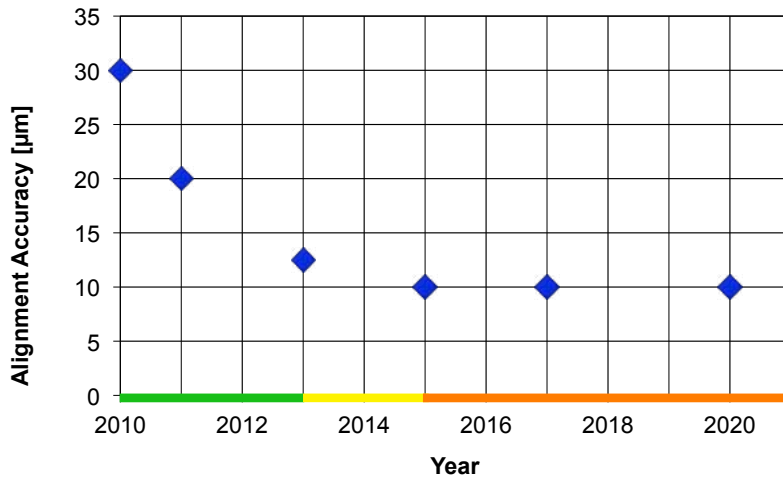


Fig. 25: Alignment precision needs to increase to 10µm (numbers are 3 sigma values).

It is crucial to get as much power out of the assembled solar cells as possible. A good parameter expressing this is the module-to-cell power ratio, defined as module power divided by cell power times number of cells (module power/cell power x number of cells). As shown in Fig. 26, this ratio is currently around 97.5% for multi crystalline silicon cell technology and 96% for mono crystalline silicon cell technology. In 2013, the power ratio will show an improvement of +1.5% abs. due to the introduction of AR glass (see Fig. 7). The introduction of new interconnection and encapsulation technologies (for back contacted cells and thin wafers) will result in a second improvement step of about +1.0% abs from 2015 onwards.

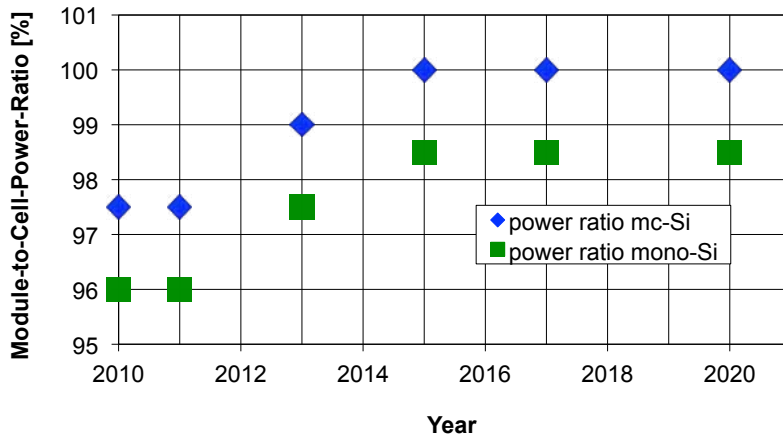


Fig. 26: Expected trend of module-to-cell power ratio.

4.3 Products

Due to the current interconnection and lamination technology, bow is an important parameter for the module manufacturer. To ensure high yields, it must be lower than 2 mm. This restriction will remain at least until 2015 when new interconnection and lamination technologies that are especially designed for handling of wafers with a thickness below 150 µm will be introduced. The cell bow restrictions for these new interconnection and lamination technologies still need to be defined. It is expected that the cell bow will decrease to 1.5 mm in 2020 due to novel cell technologies being implemented.

The share of n-type mono wafers is expected to increase over the next few years starting at about 8% today to a share of up to 50% in 2020, as shown in Fig. 27. We expect less market share for n-type multi wafers.

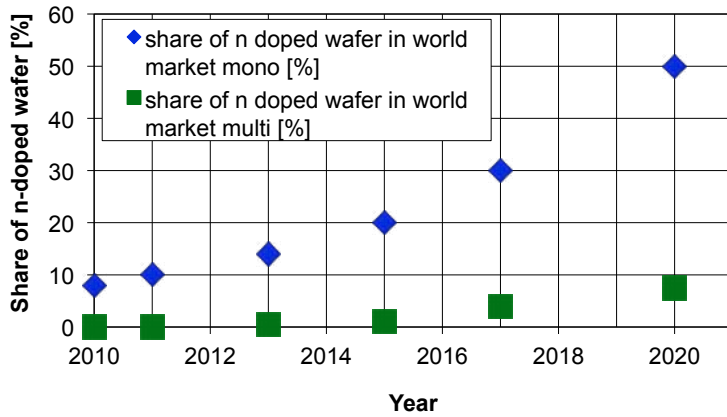


Fig. 27: Expected share of n-type material on world production of c-Si solar cells.

Over the next years, the efficiency of p-type mc-Si solar cells will increase. Fig. 28 shows the expectation of average stabilized efficiencies for mc-Si and mono-Si solar cells in a state of the art mass production line. Fig. 29 shows the corresponding development of the module power [W] considering that there will be a transition in mono-Si wafers format from semi square to full square starting in 2015.

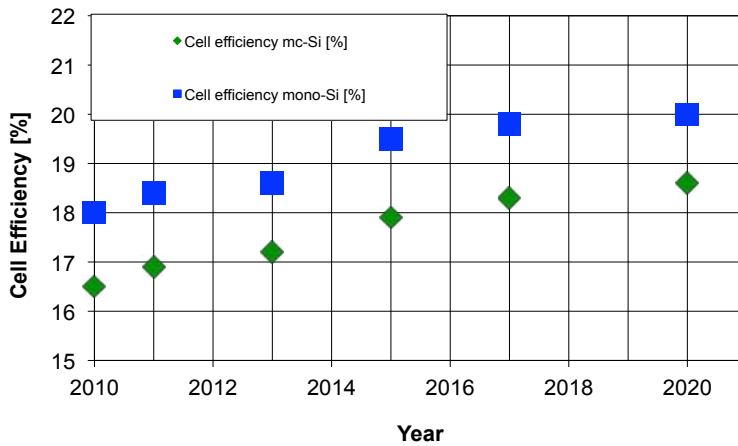


Fig. 28: Stabilized efficiency trend curve of p-type c-Si solar cells in mass production.

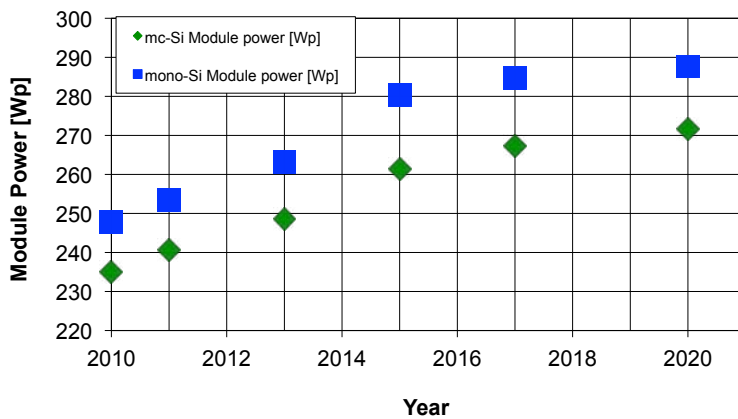


Fig. 29 Output power of 60 cell modules corresponding to the efficiency development shown in Fig. 28.

One potential way to reach higher module efficiencies and lower module production costs is to use module technology based on rear contact cells. Our forecast on the worldwide fraction of produced rear contact cells in production is shown in Fig. 30.

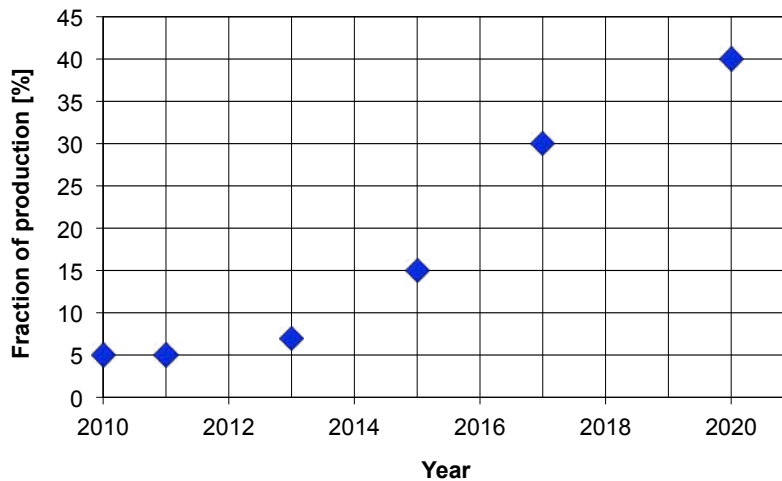


Fig. 30: Share of rear contact cells as fraction of worldwide production. We expect a strong growth in rear contact cells towards 2020.

5 Outlook

This data was collected from the leading European manufacturers along the c-Si value chain in 2010. A yearly update of this information is planned. Topics such as wafer size require cooperation between suppliers, cell manufacturers and other players along the value chain. The download of the current issue of this document as well as information about how to get involved in the roadmap activity are available on the website www.itrpv.net.

6 Acknowledgement

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About SEMI PV Group

PV Group represents SEMI member companies involved in the solar energy manufacturing supply chain. Members provide the essential equipment, materials and services necessary to produce clean, renewable energy from photovoltaic technologies. The PV Group mission is to advance industry growth, support continuous efficiency improvements and promote sustainable business practices through international standards development, events, public policy advocacy, EHS support, market intelligence, and other services.

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