Edition
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CTM Group* PV Roadmap for Crystalline Silicon

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1 Executive summary

Leading German crystalline silicon (c-Si) solar cell manufacturers (CTM Group*) have prepared a technology roadmap for c-Si photovoltaic (PV). The aim of this roadmap is to inform suppliers and customers about the expected technology developments and to set a basis to intensify the dialog about required improvements and standards.
Using the historical learning curve and the forecasted industry growth the WP costs of PV modules are expected to decrease by 8%-14% yearly. This corresponds to a significant cost reduction per cell. To reach this cost target current technology has to be optimized and between 2013 and 2015 new technologies need to be implemented in production.
In this roadmap details of requirements for c-Si solar cell manufacturing such as more effective use of material, more productive manufacturing equipment and more advanced processes are given in key parameters. This effects not only the cell production but also the whole value chain. A good example is the wafer dimension. To be able to handle thinner and larger wafers the method of producing the wafer needs to be modified, the cell process will change as well as the technology to build the module, most probably rear contact cells will be used. In case of cell size also the inverter needs to be adapted to a new current/voltage range.

To ensure a good communication with manufacturers and suppliers through the value chain, the roadmap activity will be continued in cooperation with SEMI PV Group and updated information will be published every year.

Vistit: www.itrpv.net

* The CTM Group (Crystalline Cell Technology and Manufacturing) is a Special Interest Group of Bosch Solar Energy, Sovello, Sunways, Solarworld, Schott Solar, Solarwatt, Solland, Q-Cells represented by SEMI / PV Group.

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2 Approach

To give guidance to both institutional and industrial players over the whole value chain the roadmap focuses on essential developments for long-term research. The topics are split up in three areas: materials, processes and products. In trends and graphs we show the expectation up to the year 2020 and for some parameters we indicate by color marking how we see the state of the technology today for the production chain up to the module (see table 1). Numerical values are averages of all participating companies; in their individual roadmaps some companies have higher, other lower values.

Green	Industrial solution exists and is being optimized in production.
Yellow	Industrial solution is known but not yet in production
Orange	Interim solution is known, too expensive or not suitable for production
Red	Industrial solution is not known

Table 1: Color marking

2.1 Materials

Future wafer dimension developments and material trends are described. A replacement of some materials will be necessary to secure availability, avoid environmental or health risks, reduce costs and increase efficiencies.

2.2 Processes

To reduce production costs new technologies, materials and highly productive equipment including SPC are needed. By giving information on important key figures of the production as well as details of the process to increase the cell efficiency the roadmap will be the guideline to support these developments.

Before implementation of new processes in high volume production, processes have to be proven and tools have to be qualified. History – also in other high-tech industries like the semiconductor industry- has shown that it takes about 3 years to implement a new process with new tools into production as shown in ITRS road map (Figure 1). Latest example for the implementation of a new technology in the PV industry is the implementation of chemical rear side etching as method to isolate front and rear side. To reach a stable high volume production there are two significant hurdles. First reaching a stable process on some hundred cells in an alpha phase and second some hundred thousand cells in a beta phase. Only if this has been shown, a process should be implemented in a high volume production, which means, that tool manufactures need to develop alpha tool / beta tools and qualify processes in sufficient time before introducing first production tools into the market. Therefore one has to start now to have new processes and tools in production by 2013.

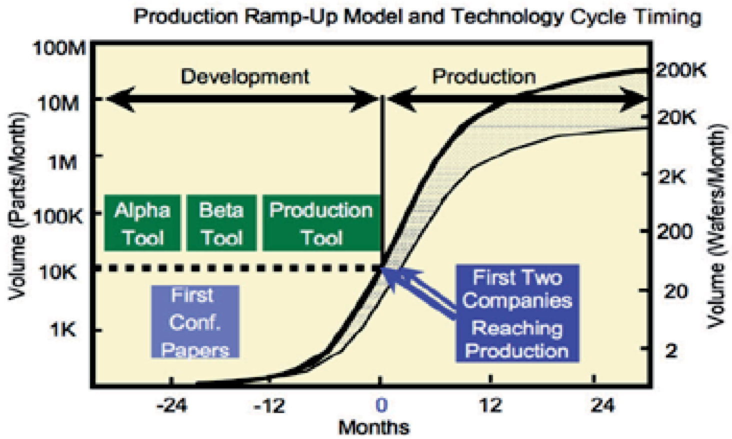

Figure 1 Typical ramp up model from semiconductor industry / ITRS, an alpha and beta tool is tested before the first two companies reach high volume production with process and production tool (ITRS).

2.3 Products

Important features of the c-Si solar cell will change over next years. Due to this fact, the roadmap will determine and take into account future wafer, cell and module developments. Issues like wafer dimension and cell architecture are defined in the roadmap.

3 Cost reduction

The overall aim of the industry is to reduce the cost of solar electricity. From empirical learning curve can be observed, that costs of solar modules are reduced about 17%-26% (learning rate) when the cumulated produced volume is doubled [F.Nemet, 2006; EPIA, 2004; Millner, 2009; Breyer, 2009].
We calculated two scenarios for the time period 2008-2020:

- scenario 1 assuming a yearly industry growth rate decreasing from 40% - 30% and a learning rate of 20% and
- scenario 2 assuming a growth rate of 50% - 40 % and a learning rate of 25%.

This leads to yearly cost reductions of 8%-9% per WP at module level in scenario 1 and 11% - 14% in scenario 2, respectively. This cost reduction can also be expected for the cell and combined with efficiency improvements from 16% up to 20%, this leads to 5%-9% yearly cost reduction per cell in scenario 1 and 8%-13% in scenario 2.
The efficiency data shall refer to 156*156 mm^2 large multicrystalline cells and corresponds with the EPIA roadmap (EPIA, 2004). This shows clearly, that the reduction of the manufacturing cost of ownership (CoO) per W_P is dominated by far by the reduction of the manufacturing costs per cell as long as the cell area is kept constant while the contribution of the efficiency increase is less pronouned. However, only a combination of an increase in cell efficiency and a significant reduction of manufacturing costs will enable the PV industry to reach the overall cost targets as depicted in Figure 2.

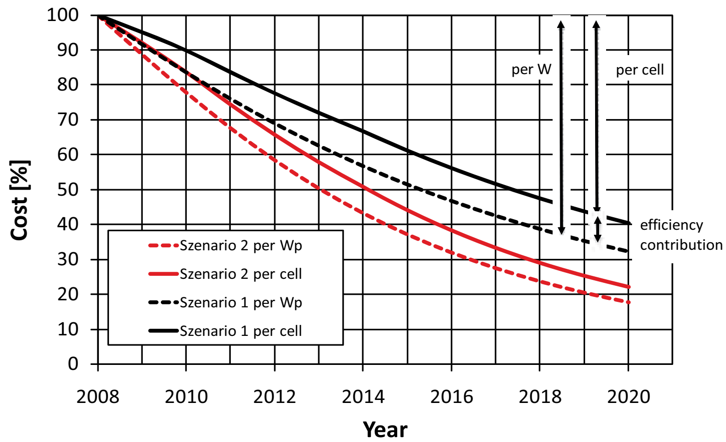

Figure 2 Cost analysis from historical learning curve. It can be seen that costs have to be reduced per piece and not only per W_P

4 Results 2009

4.1 Materials

Wafers will become thinner and larger, whereas the TTV needs to be reduced in parallel. Figure 3 shows expected average thickness reduction to 100 µm by 2020. For one individual company a step e.g. from 160 µm to 120µm due to a technology change could be also possible instead of a continuous thickness reduction. Larger wafers are expected for 2015. Methods of producing such wafers as well as tools and processes for cell and module fabrication need to be developed.

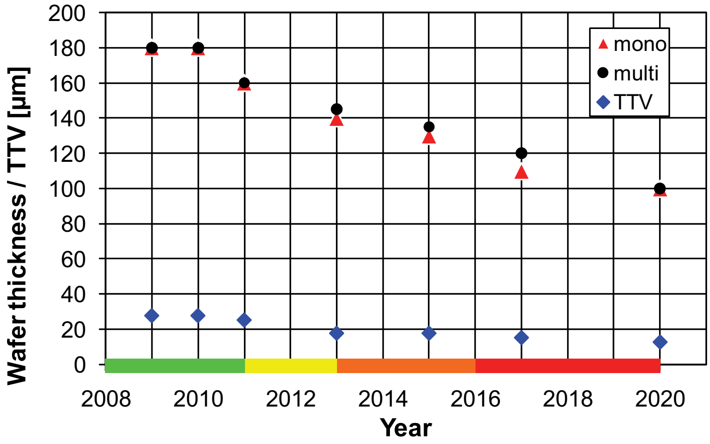

Figure 3 Wafer thickness is reduced as well as TTV.

Besides the wafer itself metallization pastes / inks are the most important materials in the cell production. In industry average, best results are obtained with pastes / inks containing heavy metals such as lead or cadmium. Without performance loss a replacement of these pastes / inks shall start as soon as possible. New materials need to be available in 2010 for qualification and testing to finish product implementation for all lines latest in 2012.

For metallization Ag is a major cost driver. Due to increasing demand, rising prices are to be expected. Therefore in a first step Ag consumption will be reduced and in a second step Ag shall be replaced within the technology change expected for the period 2013-2015.

4.2 Processes

According to the economy of scale costs of consumables need to be reduced and productivity of tools needs to be improved by increasing yield and throughput of a production line resulting in the reduction of personnel costs and tool costs per cell.

Figure 4 shows that mechanical yield loss in a fully automated production line is expected to decrease to below 1% by 2020. Note that this includes changes to thinner and larger wafer at the same time.

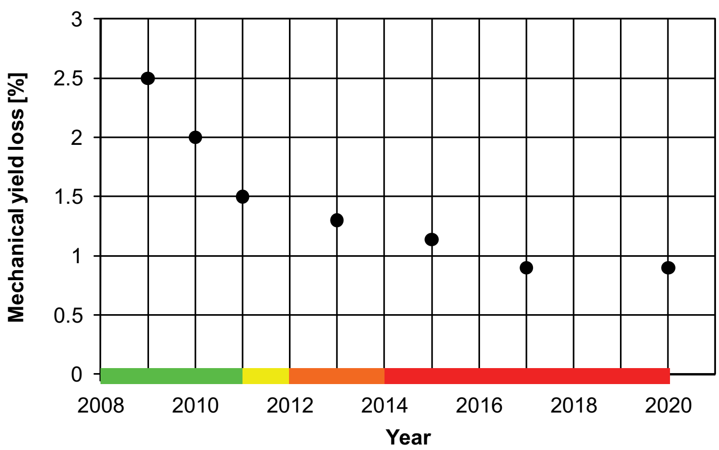

Figure 4 Mechanical yield loss needs to be reduced significantly in the next years.

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The tool uptime is another important factor for production line optimization. As shown in Figure 5 there is especially need for improvement in the process group metallization and classification to reach uptimes of beyond 96%.

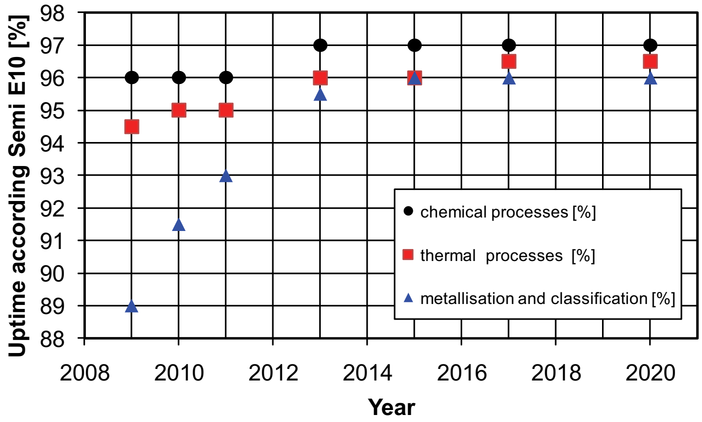

Figure 5 Tool Uptime according Semi E10 needs to be improved. There is most potential in the metallization and classification process group.

One appropriate way to reduce the tool costs per cell is to increase the throughput of the systems. Which throughput is the optimal one depends on the line concept and the cost of ownership. As a trend we show the average of the expected throughput values in table 2. To match throughput in a production line the front end (chemical and thermal processes) should have twice the throughput of the back end (metallization and classification).

Year	**Front end [wafer/h] (chemical + thermal)**	**Single line back end [wafer/h] (metallization + classification)**
2011-2012	3600	1800
2013-2015	5000	2500
2020	7200	3600

Table 2: Expected throughput of production tools. Front and back end match in 1:2 ratio.

As tool uptime and throughput is increased, the relative number of operators in relation to the line output can be reduced. We expect a reduction to about 35% up to 2020 as shown in Figure 6.

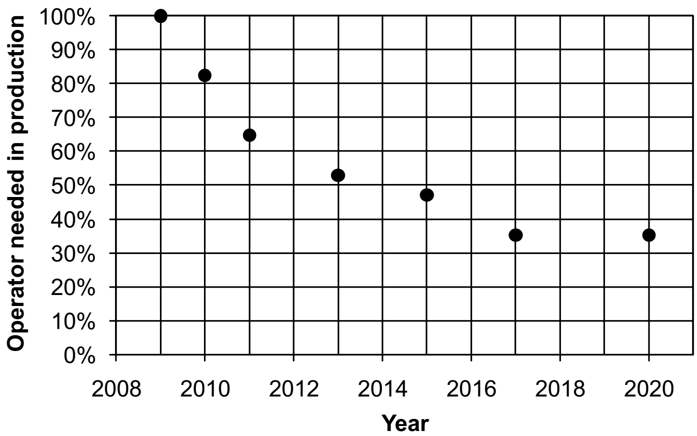

Figure 6 The relative number of operators needed in production lines can be reduced as tool uptime and throughput increases.

Besides production parameters also the cell efficiency will improve. We will name needed process parameters to achieve this improvement.

Recombination losses of front and rear side have to be reduced. It is difficult to name an easily measurable parameter. A reasonable way to describe the front surface is the emitter sheet resistance and the recombination current $J0_{front}$. Therefore we show in figure 7 the expected sheet resistance and in figure 8 the recombination current. In case of a selective emitter the sheet resistance shall refer to lower doped region whereas $J0_{front}$ includes all relevant front side parameters (emitter, surface, contacts).

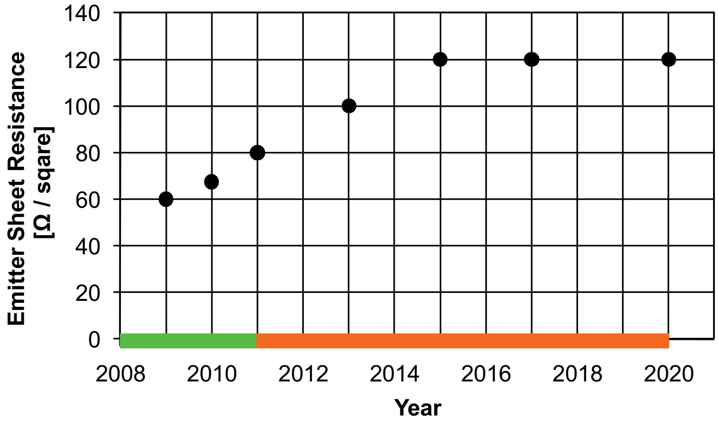

Figure 7 Emitter sheet resistance will increase.

The recombination current can be measured as described in (Kane, 1985) or it can be extracted from the IV curve, if other J0 components are known. As a first step front side will be improved, than rear side shall follow as shown in Figure 8. By 2010/2011 new processes with lower CoO than current technologies will be needed. Values below 100 fA/cm_2 cannot be reached with an Al BSF. Further more also rear side reflection has to improve.

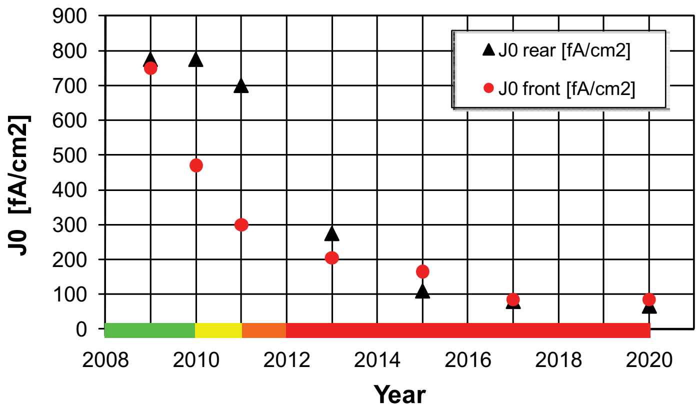

Figure 8 Recombination current J0 as parameter indicating, that first front side, than rear side need to be improved. Therefore this surface passivation needs to be improved as well as recombination in the emitter region has to be reduced.

Front metallization is a key process in production of c-Si solar cells. A reduction of the finger width without significantly lower finger resistance is needed. Further more the contact to a shallow emitter has to be guaranteed. This could be done with a selective emitter structure but it is challenging not to increase the process cost. Figure 9 shows that up to 90µm finger width seems to be feasible with current technology. From 2011 on new, more economical feasible solutions are required.

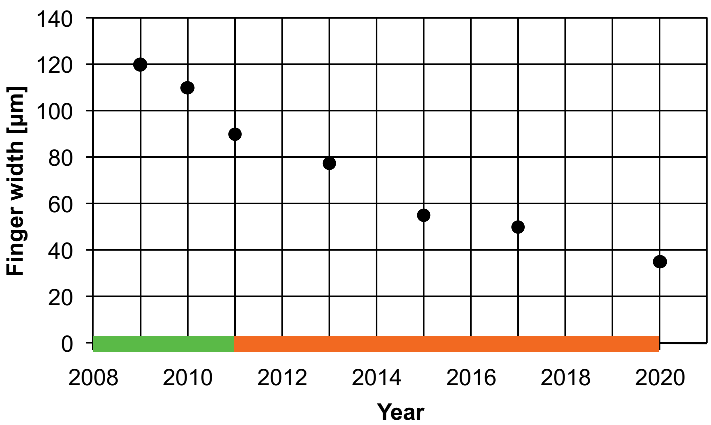

Figure 9 Finger width has to be reduced without a significant reduction of the conductivity.

Especially for the front contact it is important, that the alignment precision will improve. With current screen printing technology a tolerance of 30 µm – 50 µm can be achieved. To realize more complex cell structures the alignment accuracy should be below 10 µm as shown in Figure 10.

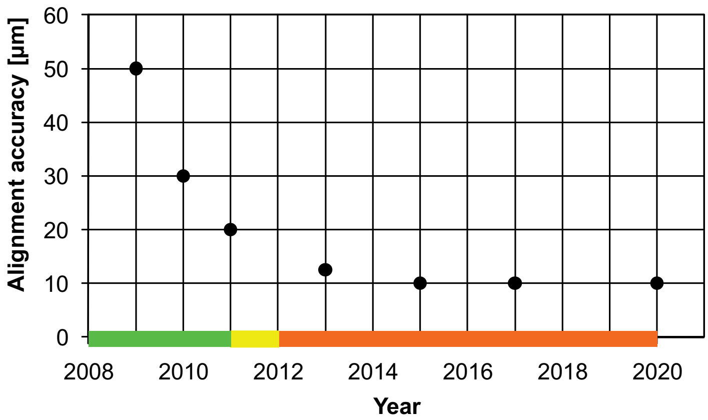

Figure 10 Alignment accuracy needs to improve to 10µm.

4.3 Products

For the current type of solar cells the bow is an important parameter for the module manufacturer. It is expected, that bow will not increase further with decreasing wafer thickness.

One option to reach higher module efficiencies and lower module production costs is module technology based on rear contact cells. The worldwide fraction of produced rear contact cells will increase according to Figure 11.

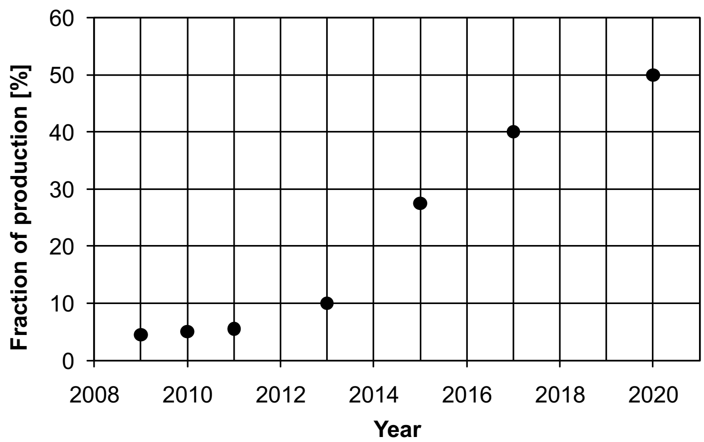

Figure 11 Rear contact cells as fraction of production. We expect a strong growth in the worldwide share of rear contact cells.

5 Outlook

This data was collected from the leading German cell manufacturers during 2009. A yearly update of the information is planned. Topics like standardization of wafer size require cooperation between wafer suppliers, cell manufacturers and other players along the value chain. To manage this best, coordination of the activity will be done by SEMI from 2010 onwards. Latest information like a download of the current issue of this document and information about possibilities how to get involved in the roadmap activity will be available on the website www.itrpv.net

An international roadmap activity is the adequate approach for the future; it took more than 6 years for the ITRS to become international. As we can benefit from the experience in the semiconductor industry we expect to reach this faster.

6 References

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