

PV Technology Roadmap Forum

June 10, 2010

ICM Munich, Germany

Panelists

Arnd Boueke

Managing Director, Sunways Production GmbH

Martin Fleuster

Director Research & Development, Solland Solar Cells BV

Ralf Luedemann

CEO, Solarworld Innovations GmbH

Axel Metz (Chair)

Research & Development, Schott Solar AG

Lars Oberbeck

Head of Solar Cell Development, SolarWorld Innovations GmbH

Peter Wawer

Senior VP Technology, Q-Cells SE

Agenda

09:00 – 09:10 Introduction & Welcome

Ralf Luedemann, CEO, Solarworld Innovation GmbH

Stephan Raithel, Managing Director, SEMI PV Group Berlin

09:10 – 09:20 Roadmap Introduction – Key Aspects

Axel Metz, Research and Development Schott Solar AG

09:20 – 09:35 The Impact of Efficiency and Scaling on the PV learning curve

Peter Wawer, Senior VP Technology, Q-Cells

09:35 – 10:20 Material (Wafer geometry and quality, Metallisation)

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European Crystalline Solar Cell Technology and Manufacturing Group (CTM)



- Open to all European solar cell manufacturers
- Contact Ralf Lüdemann or Norbert Baumbach

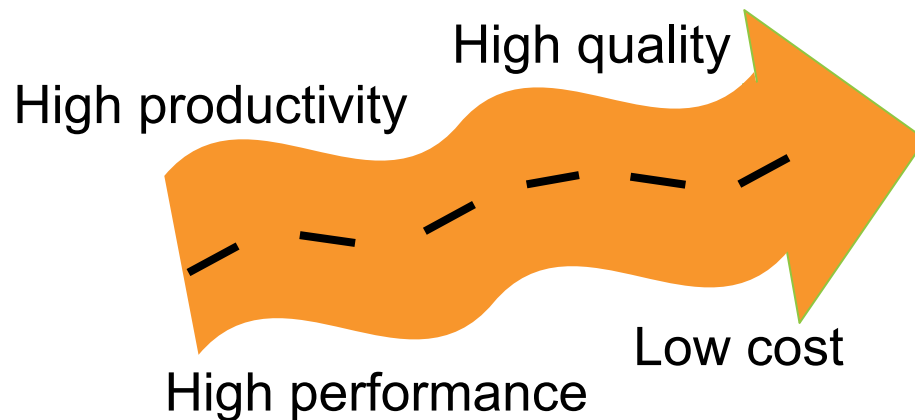
The Challenge

- Productivity (OEE, yield, W_p/worker, ...) +25%
- Performance (W/m², kWh/kW_p, ...) +40%
- Quality (Lifetime,) +100%
- Cost (€/W_p, €/kWh) -50%

→ The common goal:
A Sustainable Photovoltaics Market

European Technology Roadmap for Crystalline Silicon PV

Common path to the common goal:



Sustainable Photovoltaic Market

→ Get involved!

European Technology Roadmap for Crystalline Silicon PV

Common path to the common goal:

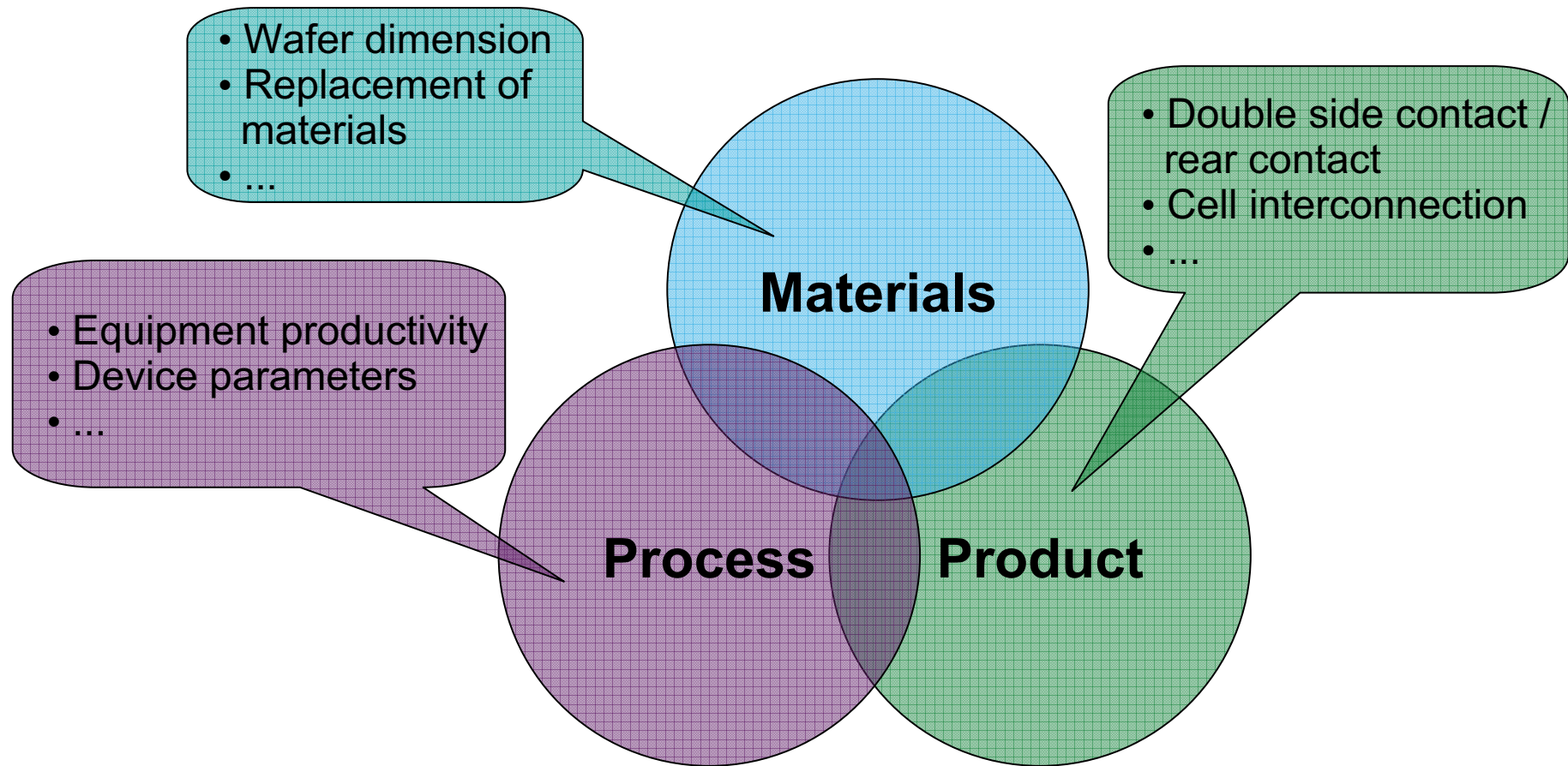
- Basis for the cooperation with our customers
 - Guideline for our material and equipment suppliers
 - Target for our technology development and R&D
- Standards will derive from the roadmap.

→ Get involved!

European Technology Roadmap for Crystalline Silicon PV

- Active work group
- Focusing on Crystalline Silicon PV value chain
- Yearly up-date and publication of roadmap
- Key technology parameters are addressed
- Your input is welcome

Approach: 3 Main Areas



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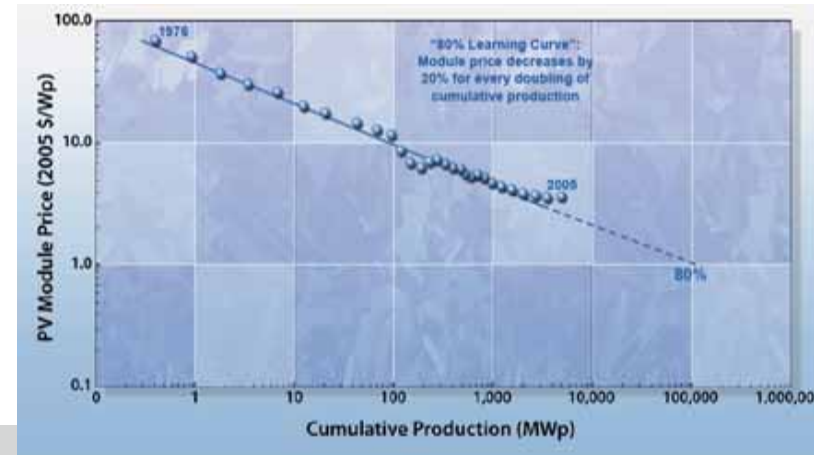
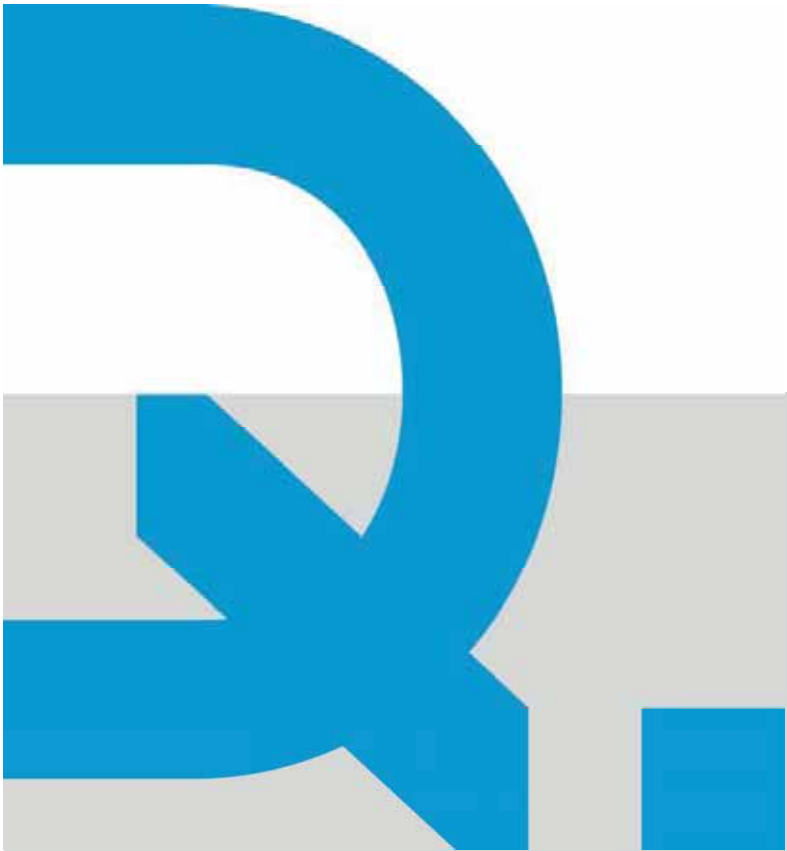
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The Impact of Efficiency and Scaling on the PV Learning Curve

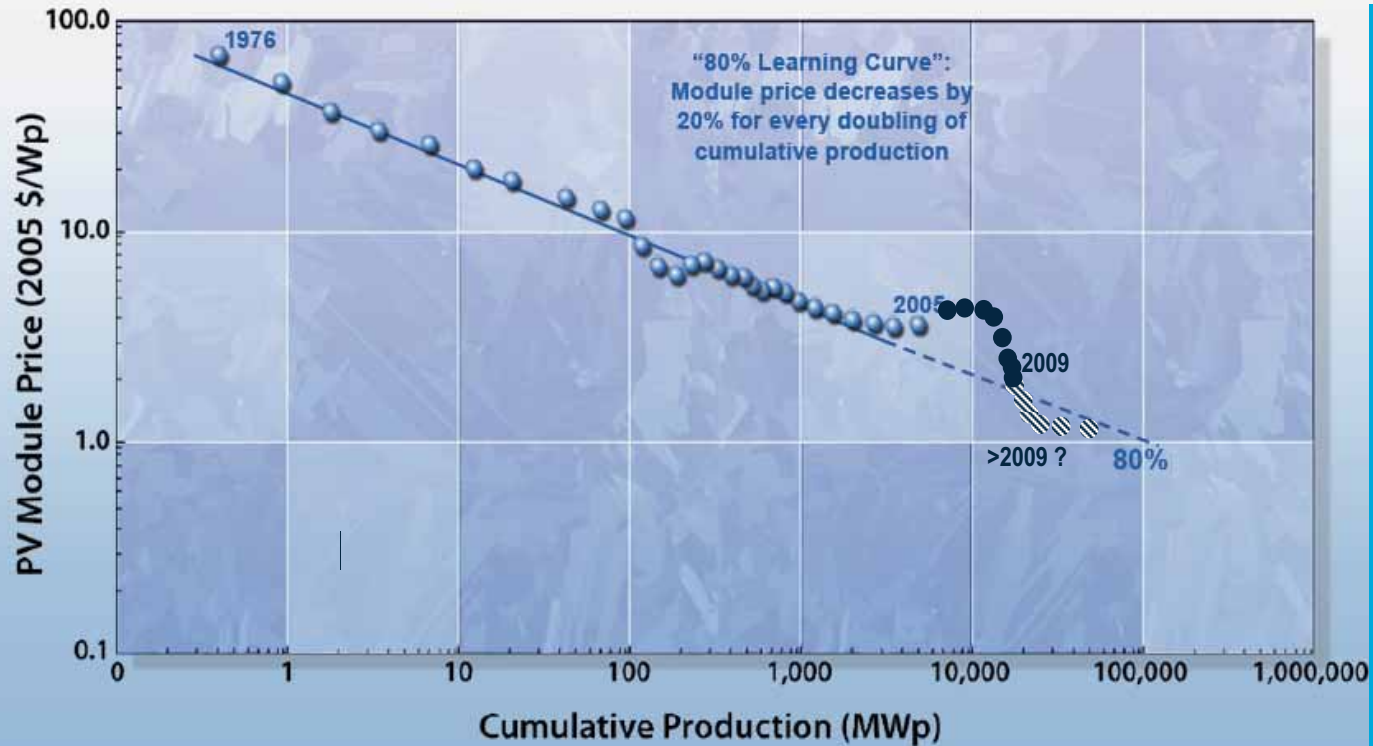
SEMI PV Technology Roadmap Forum

INTERSOLAR - June 10, 2010



PV LEARNING CURVE

PV Module Production Experience (or "Learning") Curve



PV „BACK ON TRACK“
ON
80 % LEARNING
CURVE

doubling of cumulated
production volume



-20% price reduction

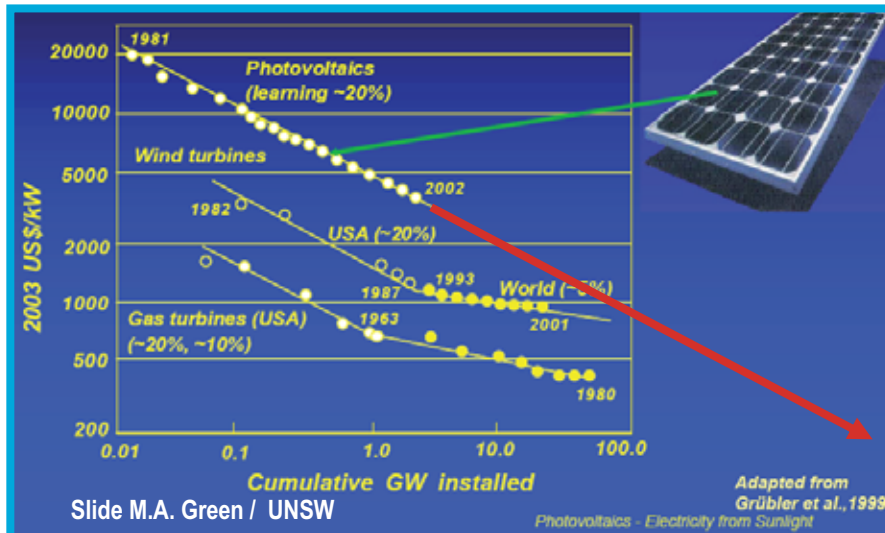
NREL National Renewable Energy Laboratory

Sources: NREL, Solarbuzz, P. Maycock, pvXchange, Morgan Stanley, New Energy Finance

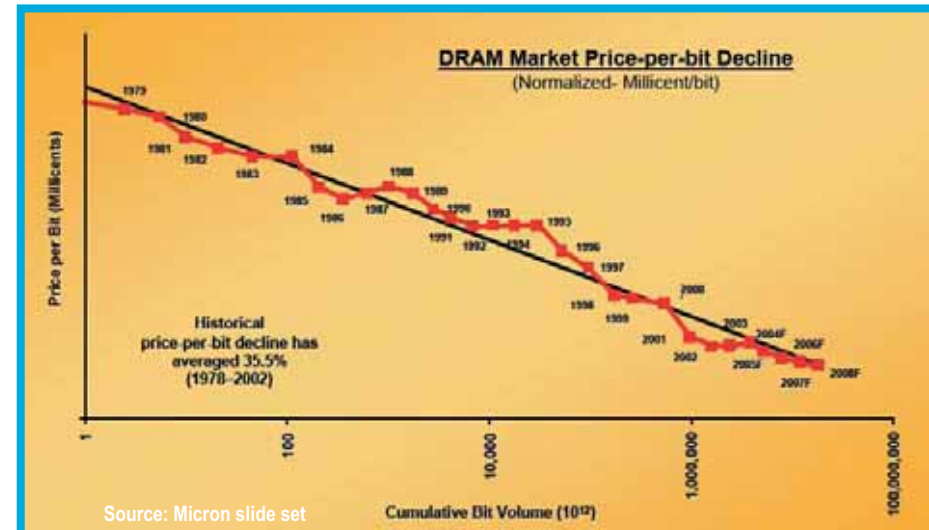


PV LEARNING CURVE

Industry Learning Curve: Photovoltaics and Semiconductor Memories (DRAM)



→ There are examples of learning curve slow down in „mechanical“ energy generation

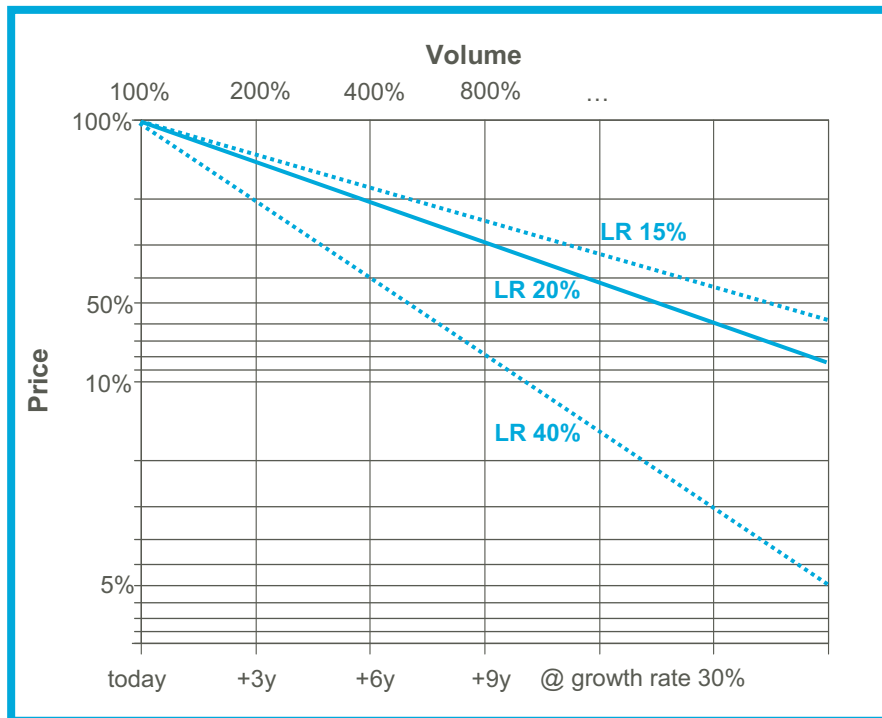


→ Semiconductors in micro-electronics run straight - over 30-40 years - in spite of being „cyclic“ and „volatile“

- Semiconductor based PV learning curve will continue to support price roadmap
- Main drivers: Technology / Scaling / Productivity

Q. LEARNING CURVE

Learning Curve: Learning Rate of Products – A comparison



learning rate	product	time frame
12 - 15 %	automobile	Ford T ...
~5% / ~35%	color TV	1960's / 1970's
17 %	glass coating	1980 - today
20 %	PV	1975 - today
28 %	broiler chicken	1934 - 1975
35 %	LCD	1995 - today
35 - 40 %	semiconductor memory	1960 - today

- Learning rates ranging from ~ 0.1 to ~ 0.4
- Growth rate determines price depression over time



PV LEARNING CURVE BREAKDOWN

Photovoltaics – Standard Screen Print Cell / Module

technical key parameter	economical parameters	
Efficiency	process complexity	scaling & productivity
<ul style="list-style-type: none"> ~ + 0,2% abs / year (historical) 	<ul style="list-style-type: none"> low process complexity 	<ul style="list-style-type: none"> Si (price & consumption) fab size other

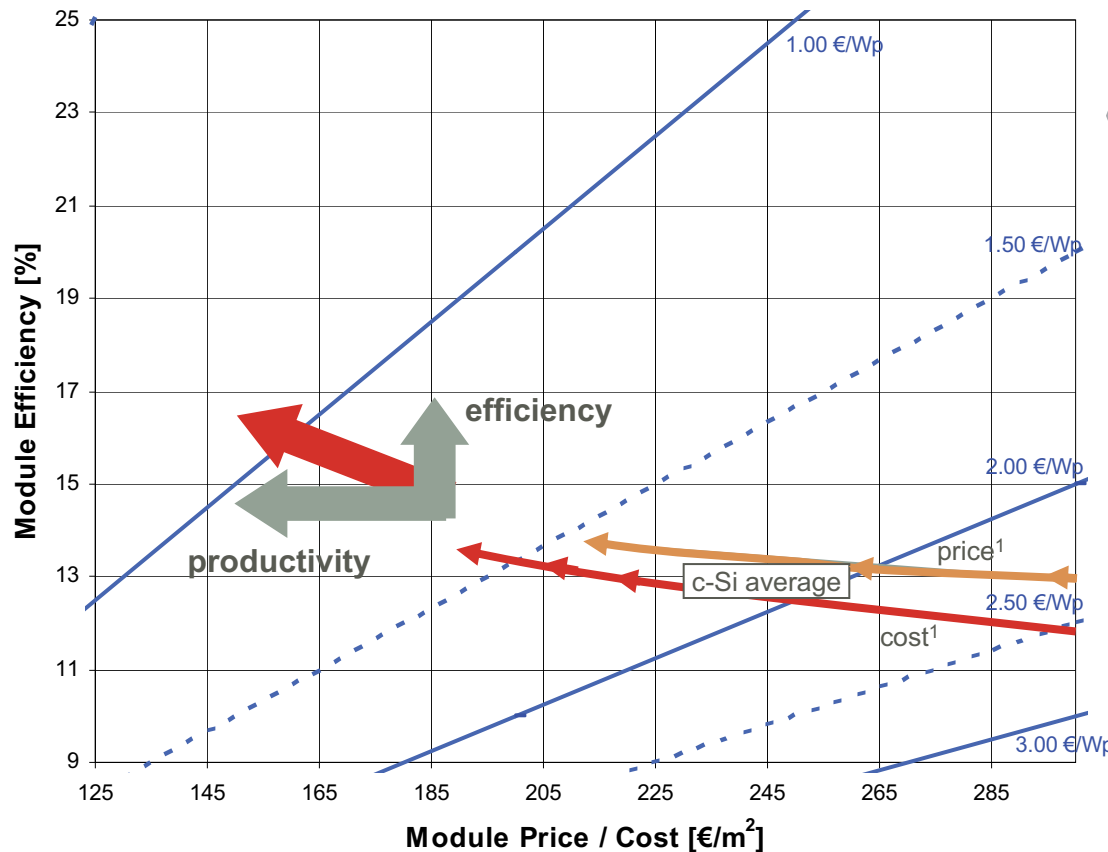
learning rate 20 %		
efficiency 3 %	area cost 18 %	
	complexity ~ 0 %	area w/o complexity 18 %
efficiency net 3 %	wafer size 3 %	15%

“If efficiency is PV’s „Moore“ efficiency & complexity will change ... ”



SOLAR MODULES: EFFICIENCY & COST

Efficiency-Cost dynamics (schematic)



- Solar electricity cost €/kWh determined mainly by
 - invest per installed system power
 - local level of solar irradiation

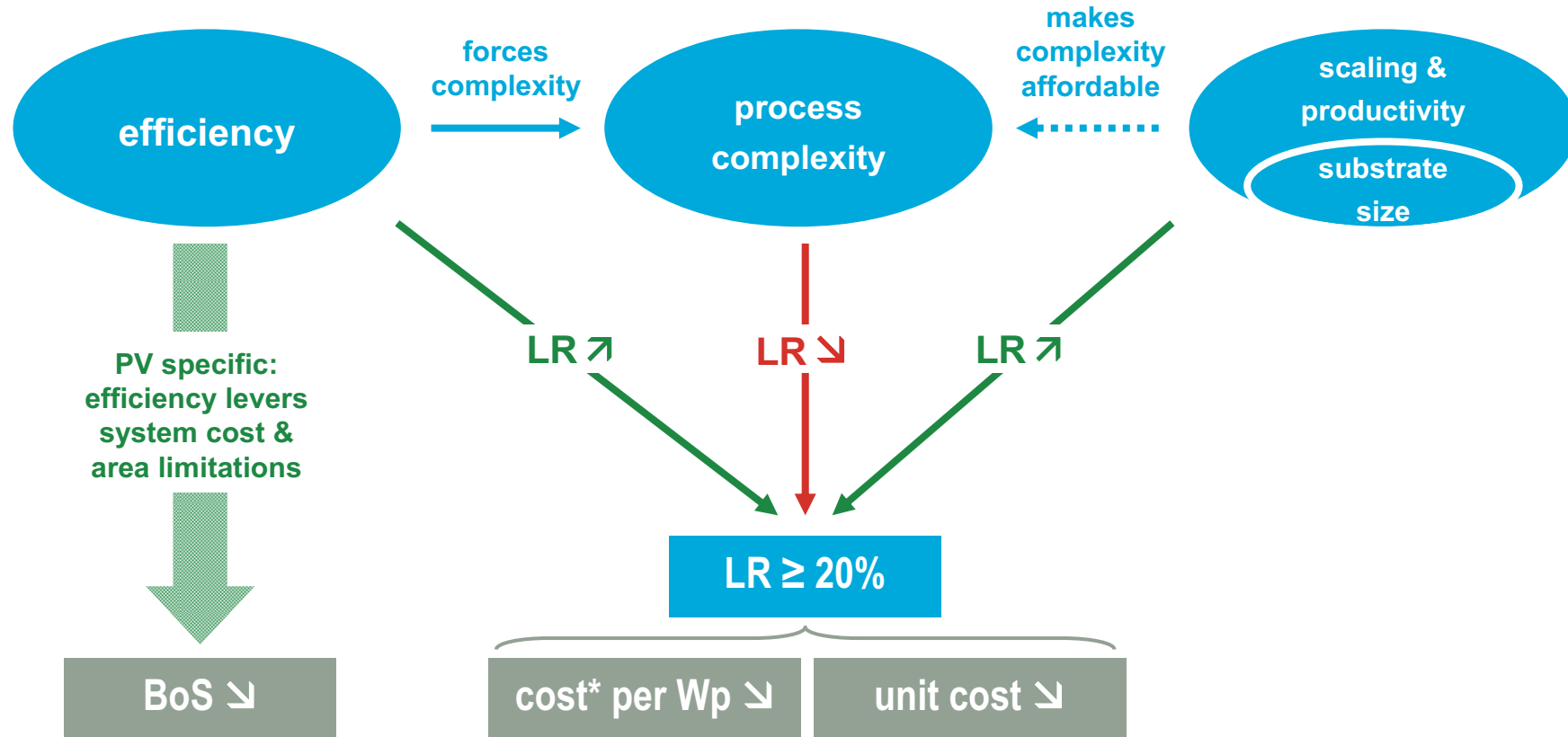
- Productivity & scaling is a major factor for cost reduction in terms of €/Wp
- Fast transfer of innovative technologies into mass production is crucial to further reduce cost

¹ avg. fully loaded Si module cost & avg. spot price Si module, Sources: Q-Cells, DB, DnBNOR, Photon Solar Updates



PV LEARNING CURVE CONTRIBUTIONS

Learning rate: key factors

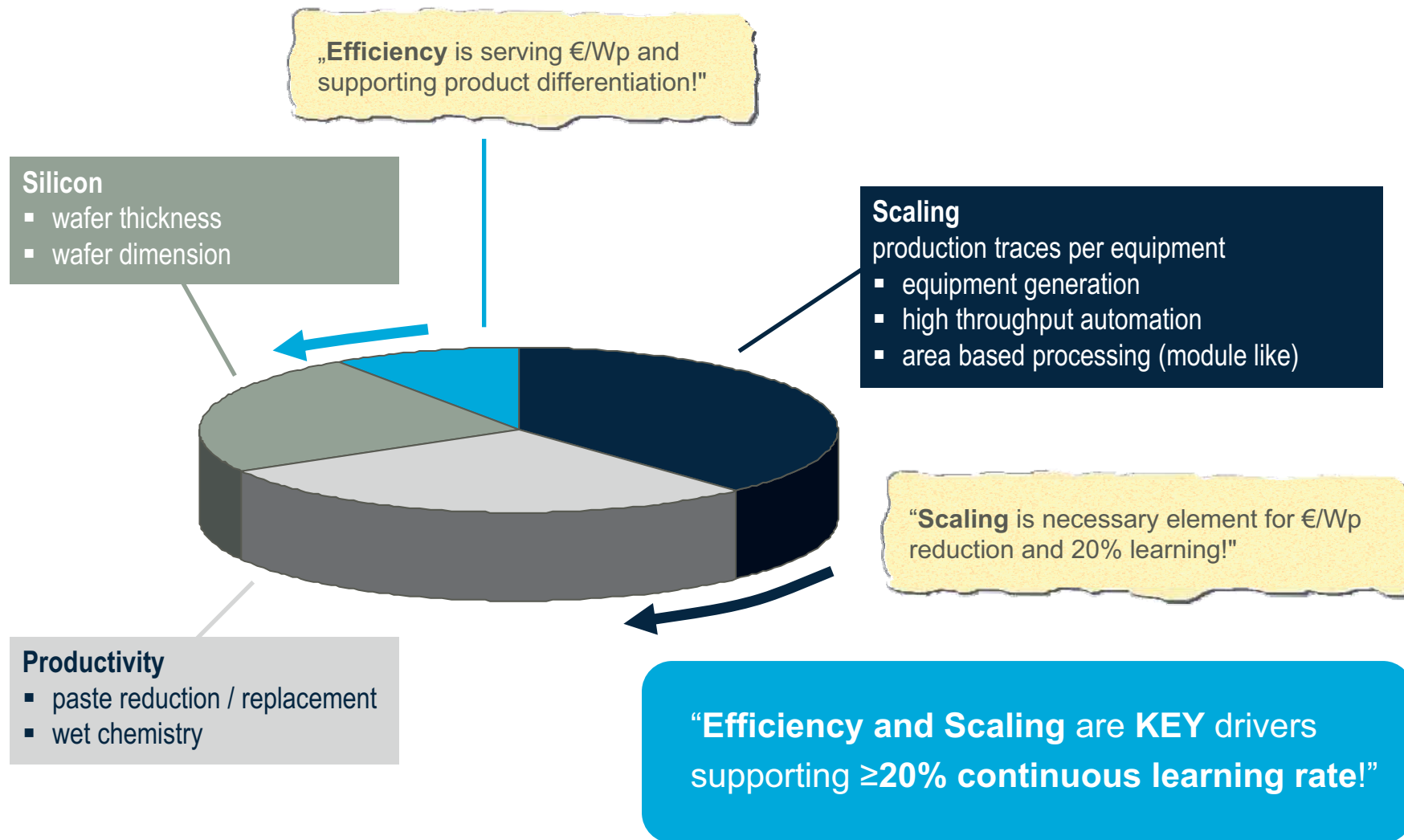


→ complex cell & module concepts need to lead to overall BoS / €/Wp / unit cost benefit

* at constant unit cost



PV LEARNING CURVE BREAKDOWN



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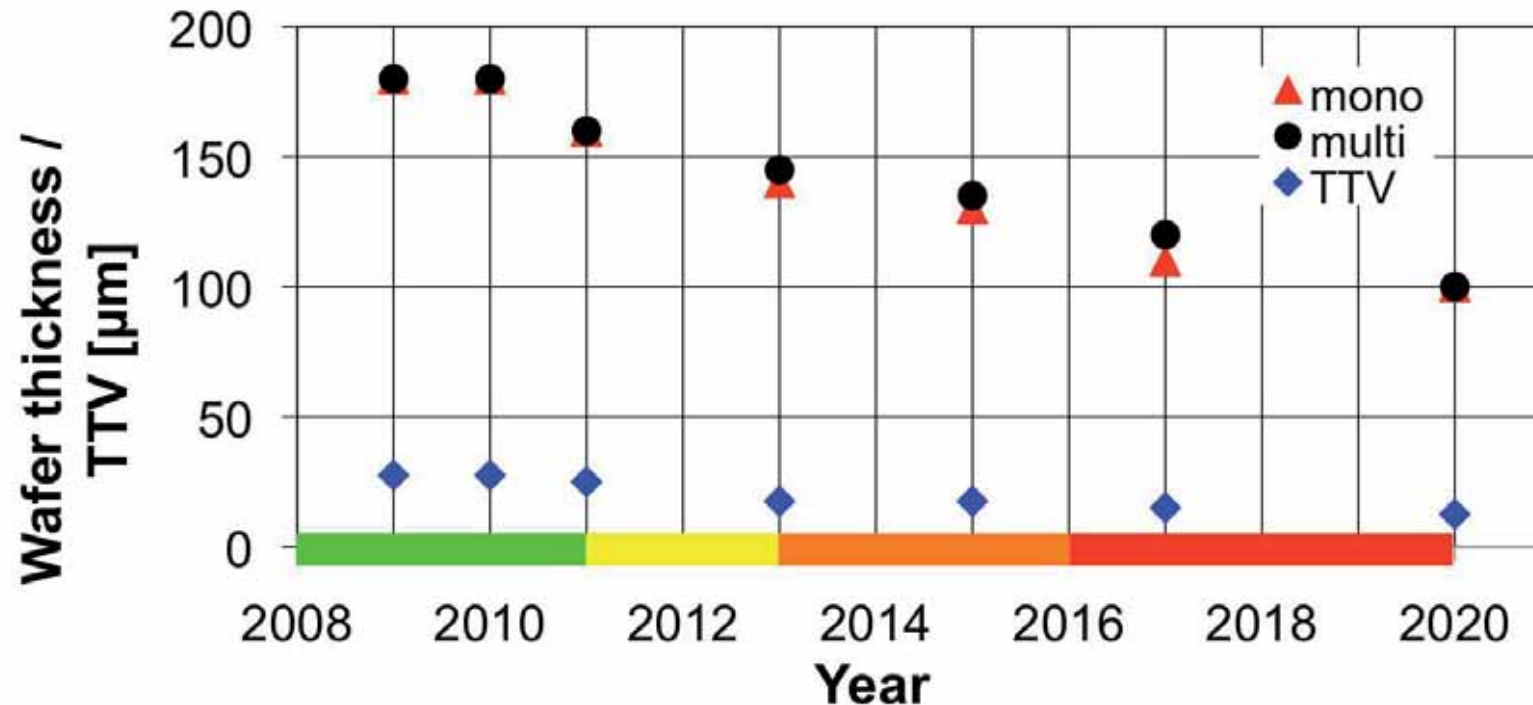
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Materials: The Roadmap predicts



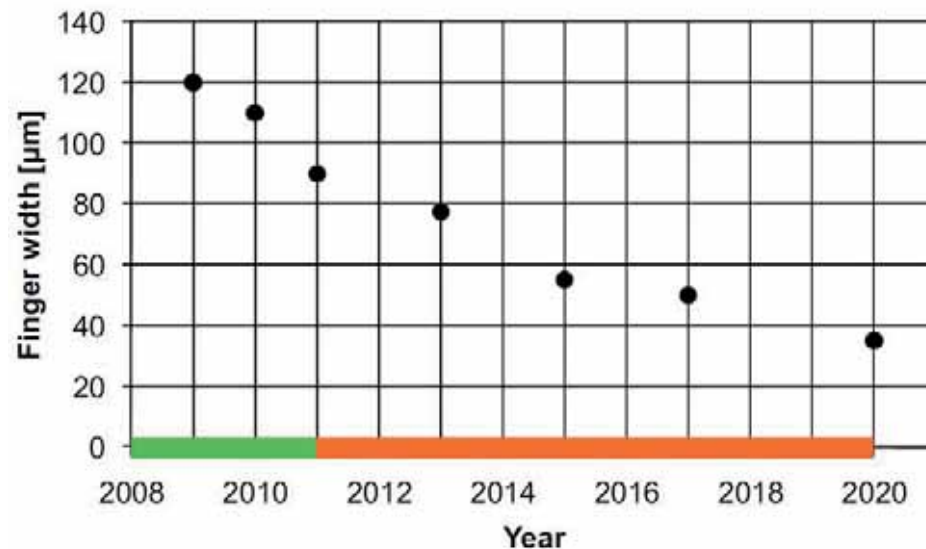
- Wafer thickness will decrease from 180 µm today to 100 µm in 2020
- Total thickness variation (TTV) will also strongly decrease
- Larger wafer size expected starting 2015

Materials: Statements

- < 180 μm thin cells require new interconnection / module technology
 - Current technology is unable to interconnect cells thinner than 180 μm
 - Reliability on module level is the most critical parameter
- Larger wafer size is only required after wafer thickness is minimized
 - Wafer thickness reduction has significant potential for cost reduction
 - Standardisation of wafer size mono/multi (125 mm, 156 mm, 2XX mm)
- Wafer quality has to be improved to further increase cell efficiencies
 - Quality parameters (electrical + mechanical) have to be defined
 - Capable inline measurement systems are required

Metallization: The Roadmap predicts

- Need for lead-free metallization pastes / inks without performance loss in 2010 for qualification, implementation in production 2012 latest
- Ag paste / ink is major cost driver → need to reduce CoO
 - decrease Ag consumption now
 - replace Ag by alternative metal in 2013 – 2015



- Drastic decrease of finger width and alignment accuracy necessary

Metallization: Statements

- Major additional efforts from paste / ink suppliers needed:
 - Performance of lead-free pastes still lower compared to lead containing products
 - High-ohmic emitters need to be contacted reliably
 - Need to have more uniform height profile of screen-printed fingers for reduced paste consumption
 - Strong potential for improved rear-side metallization: better BSF and reflection, decreased film thickness, lower bow
- Is screen-printing a suitable technology for achieving finger width $<60\mu\text{m}$?
 - Strong need for investigation of alternative techniques now

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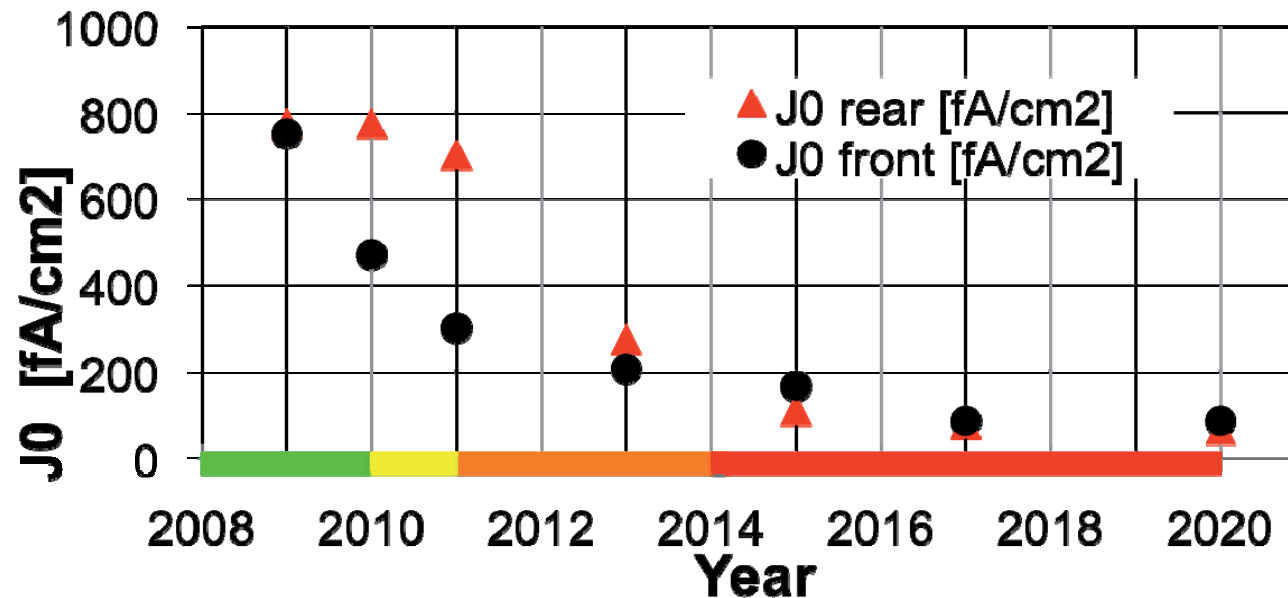
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Process: the roadmap predicts

- Higher sheet resistance and better passivation leads to reduced recombination on front- and rear-side



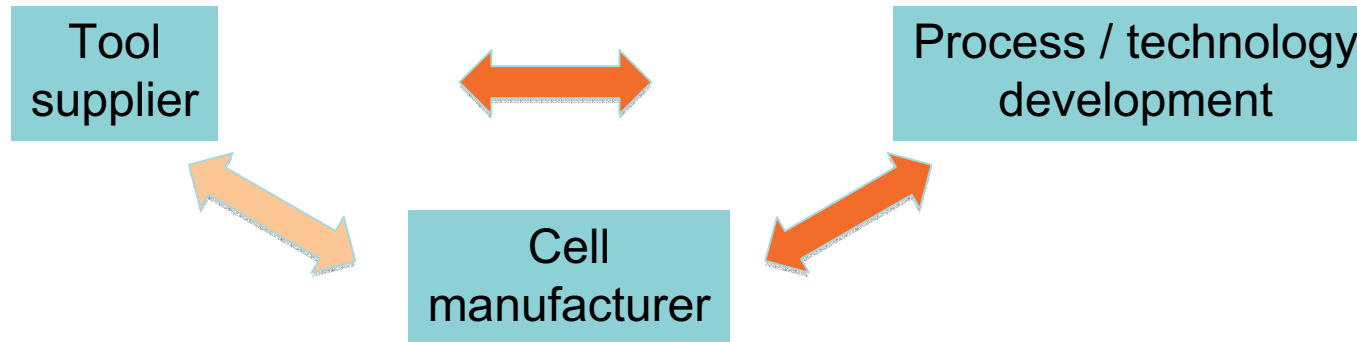
with lower
CoO

- Emitter sheet resistance will increase to 100 Ohm/sqr. in 2013
- Reduction of finger width to 75μm in 2013
- Alignment accuracy decreases to 12μm in 2013

Process: Statements

- Equipment manufacturers are not able to provide the required technologies concerning improvements in J_0 rear ($<300\text{fA/cm}^2$ in 2013)
 - with lower CoO (and lower cost per piece)
 - with increasing throughput
 - as a qualified production tool (not α -tool)
- Pastes to contact a 100 Ohm/sqr emitter will be available too late for production in 2013
 - Pastes must be available in Q3/2011 for testing on cell level and certification of the modules (> 9 months)

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- Process development is done by cell and tool supplier
→ Conflict of interest concerning IP
- two possible ways:
 - a) strict separation of hardware and process – recipes
 - b) cooperation between tool supplier and cell manufacturer
(benefit for cell manufacturer?)

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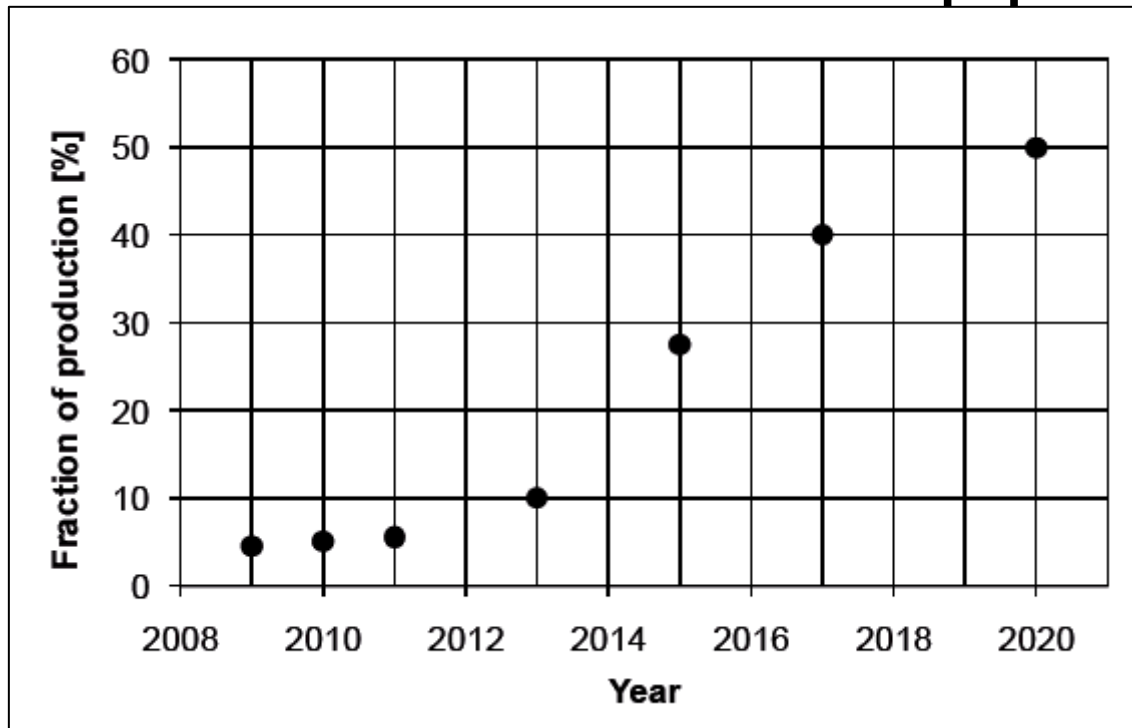
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Product: The Roadmap predicts



Share of back-contact cells of total production volume

- Strongly increasing share of back contact cells from 2013 onwards
- Wafer thickness will strongly decrease
- Bow will stay at 2008 level, at decreasing wafer thickness
- Contact layout (busbars): Standardization necessary

Product: 3 Statements

- The present module technology leads to a dead end!
 - Unable to handle cells thinner than 180 μm
 - Unable to profit from the intrinsic efficiency potential of back-contact cells
- We will see a strong trend towards integration between cell and module technology
 - Introduction of new concepts only possible in an integrated approach (present module makers block progress)
 - The border between cell and module processing will stepwise disappear
- There is no need for standardization of contact lay-out
 - Not needed by future technology
 - Design freedom needed to optimize module efficiency (per cell concept)

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